Fawad 13820

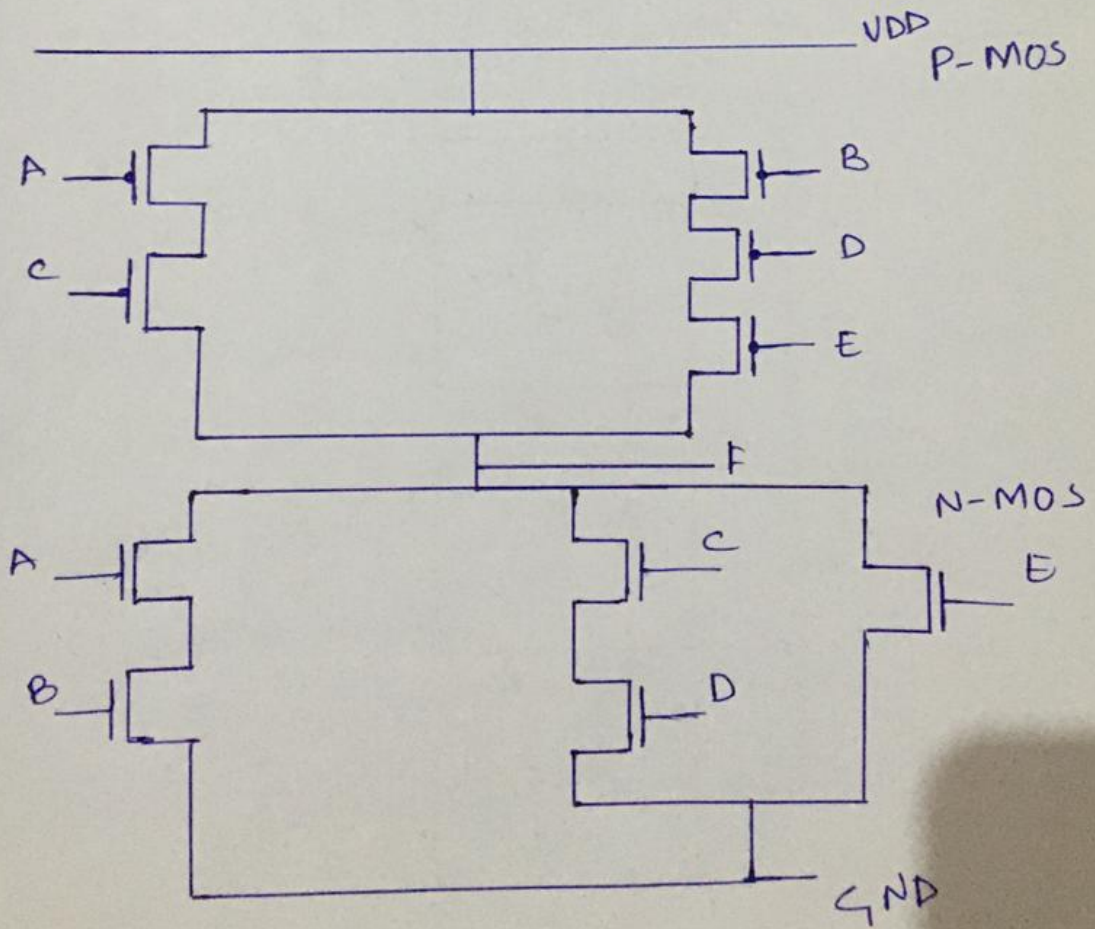
Q1: Design an area effect layout diagram for cMOS logic;

$$F = AB + (C + D)E$$

Ans:

N = • series
+ parallel

P = • parallel
+ series



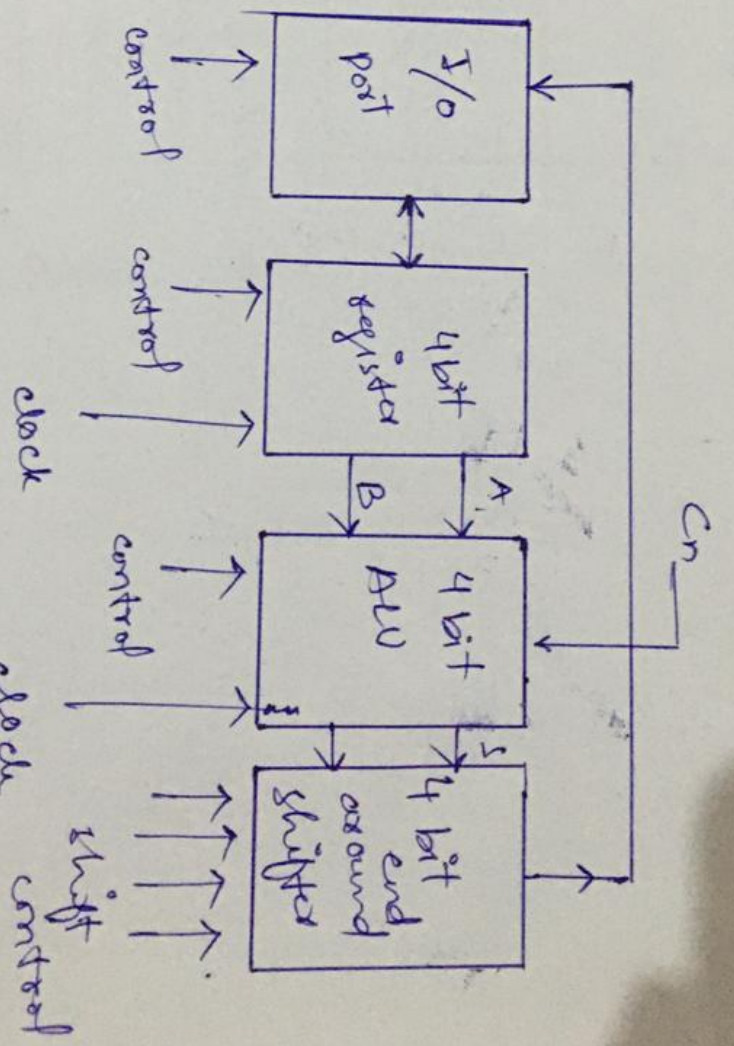
Fawad

13820

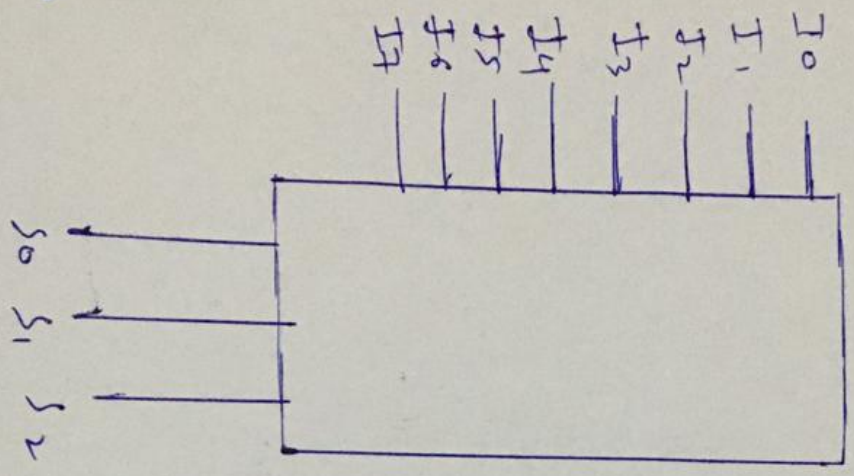
Q2: Subsystem design consideration of four-bit adder.

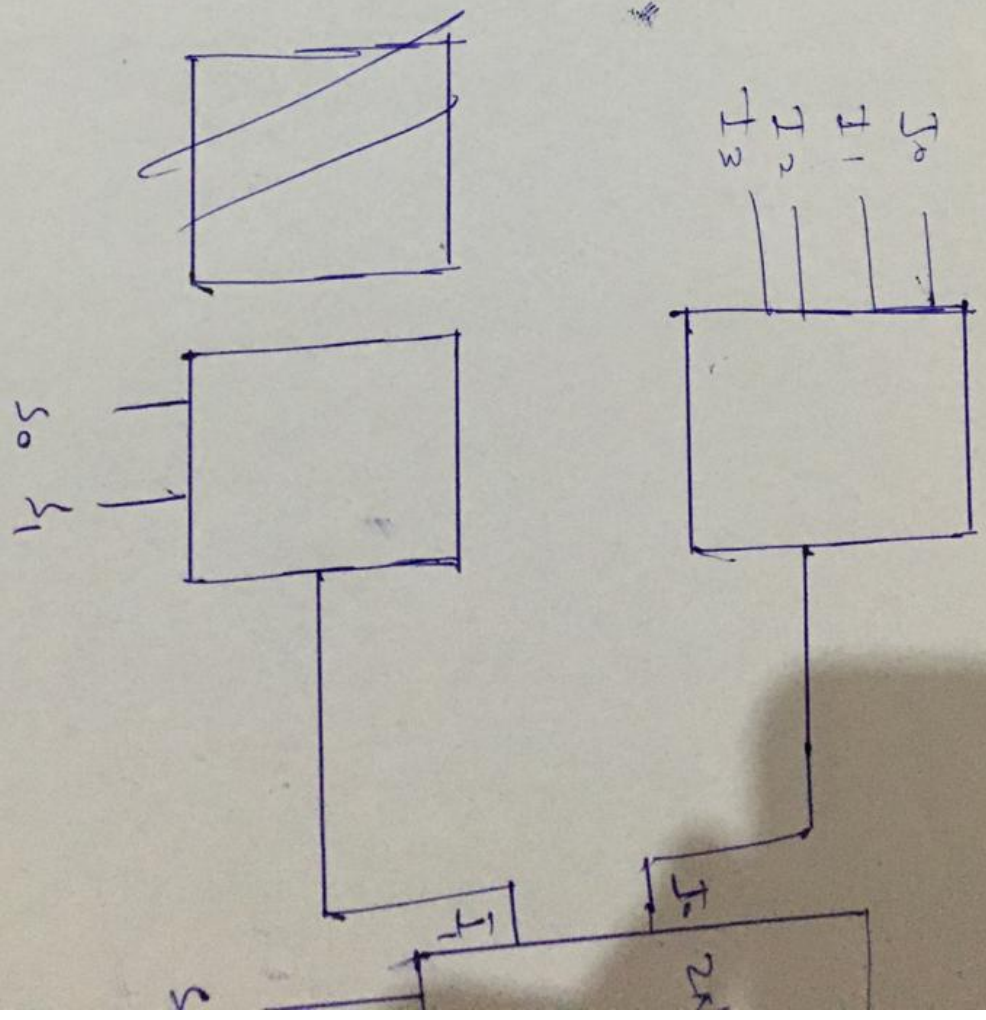
Ans:

Now I want to design a subsystem design consideration of four-bit adder.



Q5 Ans 6





Fawad 13820 (8)

Q4 Ans: Inverter have always lower limit of power depends on sum of NMOS & Vdd

→ Logic funct is implemented
→ Full swing output
→ faster switching speeds

Fawad 13820

Q3(B): Simple parity check code?

Ans: A parity check code is the process that ensures accurate data transmission b/w node during communication

E.g:

⇒ Sequence Even bit

0100010
1000000

⇒ Even parity Bit

01000100
1000001

⇒ Odd parity bit

01000101
1000000

(5)

⇒ VLSI design Trend

Fawad
13820

→ Trend in design & manufacturing of very large scale integrated ckt shows towards smaller cmos wafer dimension has become prevailing due to its high speed & packing coupled with low power.

→ Several trends processor, memory, iso devices TN, Hardware & Software

Fawad 13820 (4)

Q3 = VLSI Issues & Design trends:

Ans =: First of all I want to discuss about VLSI design issues;

⇒ Realize a given specifications on silicon, optimizing the following

→ Area
→ Power dessipation
→ speed
→ design time
→ testability

→ Optimization cannot be done in one step
→ partition problem & Optimize

⇒ Fawad 13820 (3)

Design of 4bit adder;

Inputs			Outputs	
P_K	B_K	C_{K-1}	S_K	C_K
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

From table one form of equation is;

Sum;

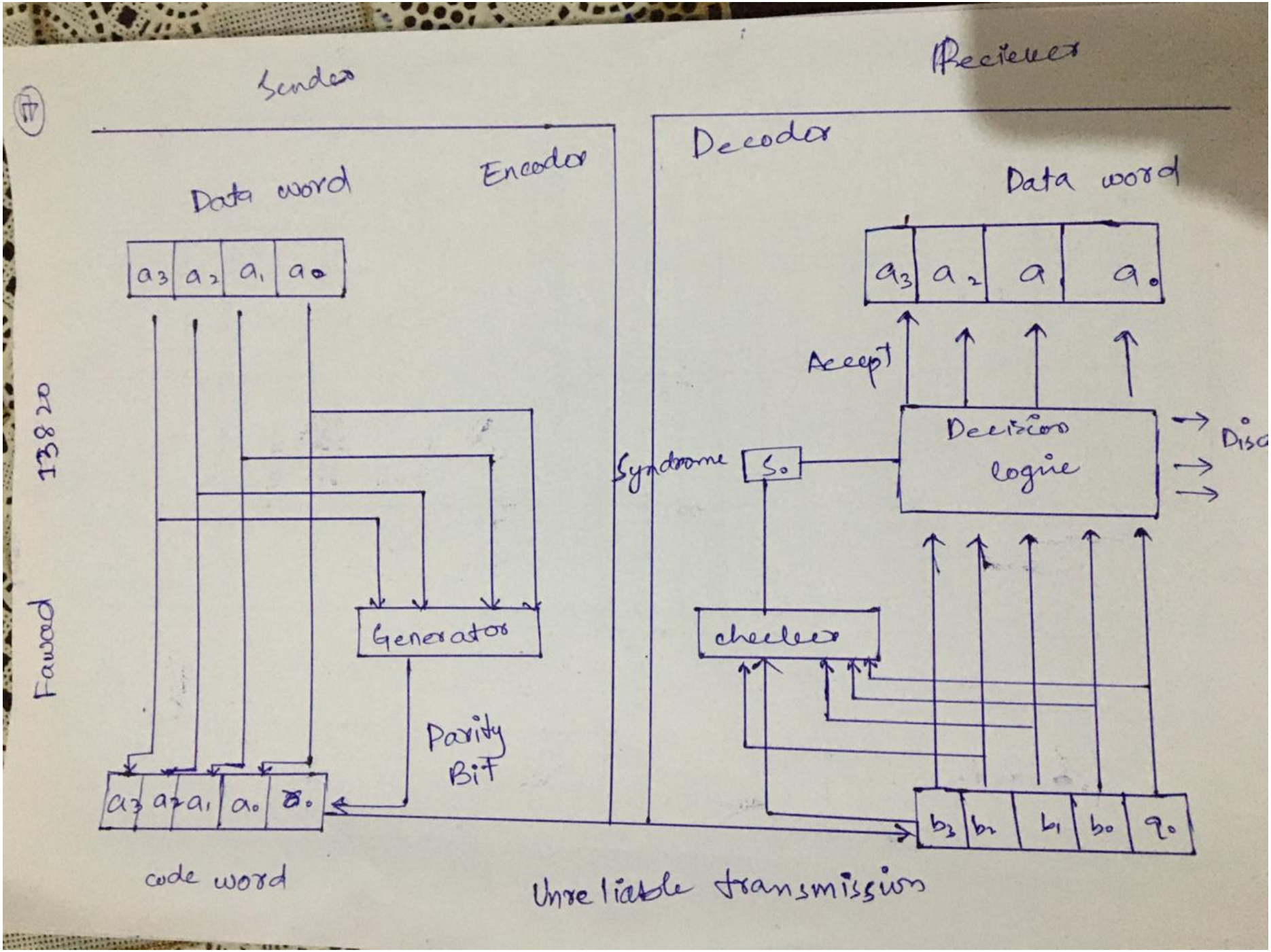
$$S_K = H_K C_{K-1} + H_K^3 C_{K-1}$$

Now carry;

$$C_K = A_K B_K + H_K C_{K-1}$$

where half sum;

$$H_K = A_K^2 B_K + A_K B_K^3$$


Sender
Reciever
Encoder
Decoder
Data word
Data word
a_3 a_2 a_1 a_0
q_3 a_2 a q_0
Accept
Decision logic
Syndrome
S_0
Generator
checker
Parity Bit
a_3 a_2 a_1 a_0 π_0
b_3 b_2 b_1 b_0 q_0
code word
Unreliable transmission
Fawad
13820

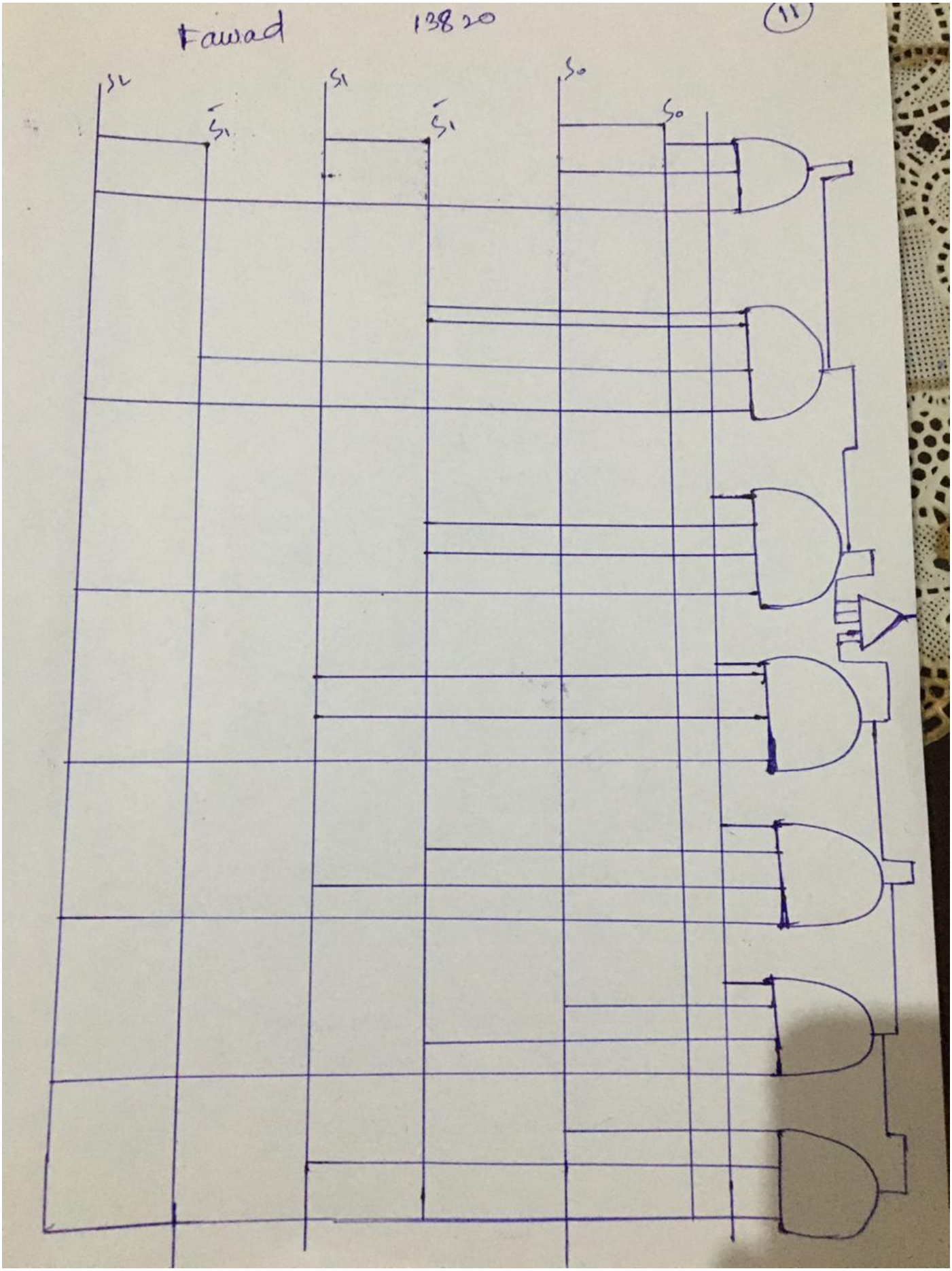
Fawad 13820

S_2	S_1	S_0	output
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

4×1		
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

2×1		
S_1	S_0	Y
0	0	I_0
0	1	I_1

Fawad 138120



⇒ 8x1 mux by VOL method

$I_0 = \bar{S_2}\ \bar{S_1}\ \bar{S_0}$

$I_1 = \bar{S_2}\ \bar{S_1}\ S_0$

$I_2 = \bar{S_2}\ S_1\ \bar{S_0}$

$I_3 = \bar{S_2}\ S_1\ S_0$

$I_4 = S_2\ \bar{S_1}\ \bar{S_0}$

$I_5 = S_2\ \bar{S_1}\ S_0$

$I_6 = S_2\ S_1\ \bar{S_0}$

$I_7 = S_2\ S_1\ S_0$