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(Q.1)

Give answer to each of the following:

(A)

What are the four main function of a Computer?

Ans:

① Data Processing:-

Data may take a wide variety of forms and the range of processing requirements is broad.

② data storage:

The Computer performs a long-term data storage function. files of data are stored on the computer for subsequent and update.

③ Data Movement:

When data are moved over longer distance to or form a remote device, the process is known as data communication.

④ Control:

Within the Computer a Control unit manages the Computer's resources and orchestrates the performance of its functional parts in response to instructions.

"B".

figure 01 Shows the IBM zEnterprise EC12 core layout Briefly explain the function of each sub-area.

ANS:

- ISU (Instruction Sequence unit):

Determines the sequence in which are instructions are executed in what is refered to as a Superscalar architecture.

- IFU (Instruction fetch unit): Logic for fetching instructions.
- IDU (instruction decode unit):

The IDU is fed from the IFU buffers, and is responsible for the parsing and decoding of all z/Architecture operation codes.

- LSU (load store unit):

it is responsible for handling all types of operand accesses of all lengths, modes, and forms formats as defined in the z/Architecture.

- XU (translation unit):

This unit translates logical addresses from instructions into physical addresses in main memory. It Contains TLB used to speed up memory access.

- FXU (~~binary~~ fixed-point unit):

The FXU executes fixed-point arithmetic operat

- BFU (binary floating-point unit):-

The BFU handles all binary and hexadecimal floating-point operations, as well as fixed-point multiplication operations.

- DFU (decimals floating point unit):

The DFU handles both fixed-point and floating-point operations on numbers that are stored as decimal digits.

- RU (recovery unit):

The RU keeps a copy of the complete state of the system that includes all registers. Collects hardware fault signals.

- COP (dedicated co-processor):

The COP is responsible for data compression and encryption functions for each core.

- I-Cache: This is a 64-KB L1 instruction cache allowing the IFU to prefetch instructions before they are needed.
- L2-Control:

This is the control logic that manages the traffic through the two L2 caches.

- Data L2: A 1-MB L2 data cache for all memory traffic other than instructions.
- Instr-L2: A

A 1-MB L2 instruction cache:

(4)

"C"

Ans:- The IAS operates by respectively performing an instruction cycle. Each instruction cycle consists of two sub-cycles.

Fetch cycle:-

The opcode of next instruction is loaded into the IR and the address portion is loaded into the MAR. This instruction may be taken from the IBR or it can be obtained from memory by loading a word into the MBR and then down to the IBR, IR and MAR.

Execute cycles:-

The control circuitry interprets the opcode & executes the instruction by sending out the signals to cause data to be moved or an operation to be performed by the ALU.

"D"

Ans:-

(a) No these programs are never considered to be embedded because they are not an integral components of a larger system.

(b) yes register are regardless what the disk drive is used for the software within the disk drive control the HDA hardware and is hard real time as well.

(e) No input-output devices. do not represent the embedded System

(d) Yes PDA is an embedded System because it just like a personal computer in hand.

(e) yes the, firmware in the cell phone is controlling the radio hardware.

(f) Yes these Computer were generally some of the most powerful Computers available when the system was build built and located in a large computer room occuping almost one whole floor of a building and may be hundreds of meters away from the radar hardware. the Software running in these Computer Controls the radar hardware. there fore the computer are an integral Components of a large System.

(g) If the FMS is not connected to the avionics and is used only for logistics Computerizations a function readily performed on a laptop then the FMS is clearly not one embedded.

(h) Yes both in the Simulator and in the things being are tested in the HIL Simulator hardware is being Controlled on both sides.

(i) yes. in this case of the "System" is the Combination of the pacemaker and the person's heart.

(j) yes. it is part of a large System. the engine, and it is directly monitoring and Controlling the engine through Special hardware.

(Q2)

A. Main Structural Components of a Computer.

Ans: There are four main Structural components of a computer

① Central processing unit: Control the operation on the Computer and performs its data processing function often Simply referred as processor.

② Main Memory: Store data.

③ I/O: Moves data between the Computer and external environment.

④ System interconnections: Some machine are that provide to communication among CPU main memory and I/O.

"B"

key characteristics of a planned Computer family.

ANS: The characteristics of a family are as follows.

- Similar or identical instruction Set:-

In some case the lower and end of the family has an instruction Set that is a subset of that of the top end of the family This mean that Program Can move up but not down.

- Similar or identical operating System: The same basic operating system is avalble for all family members.
- Increasing Speed: The rate of instruction execution increases in going from lower to higer family members
- Increasing number of I/o ports:- The number

of o/d ports increases in going from lower to higher family members.

- Increasing memory size:- The size of main memory increases in going from lower to higher family members.
- Increasing cost:- At a given point in time, the cost of a system increases in going from lower to higher family members.

"C"

Stored program computer.

Ans:- A fundamental design approach first implemented in the IAS computer is known as the Stored-program concept. This idea is usually attributed to the mathematical John von Neuman.

The first publication of ideas was in a 1945 proposal by von Neuman for a new computer the (EDVAC) in 1946 von Neuman and his colleagues began the design of a new Stored-program computer referred as the IAS computer as the princeton institute for Avanced studies.

it consists of.

- A main memory which stores both data and instructions.
- An arithmetic and logic unit capable of operating on binary data.

(D. Moor's law)

The famous Moore's law which was proponded

by Gordon Moore Cofounder of intel, in 1965 [MOOR65] Moore observed that the number of transistor that could be put on a single chip was doubling every year.

The consequences of Moor's law are profound.

1. The computer cost logic and memory circuitry has fallen at a dramatic rate.
2. Because logic and memory elements are logical and memory elements are close together more speed.
3. The computer becomes smaller making more convenient to place in a variety of environment.
4. There is a reduction in power requirement.
5. with more circuitry on each there are fewer Interchip Connections.

(Q3)

A. Computer organization and Computer architecture.

- Computer architecture:

refers to those attributes of a systems visible to a programmer or put another way those attributes that have a direct impact in logical execution of a program.

- Computer organization:- refers to the operational units and their interconnection that realize the

the architectural Specifications. Examples of architectural attributes include the instruction Set the number of bits used to represent for addressing memory.

B. (Risc and Cisc.)

- The current x86 offering represent the result of decades of design effort on (CISCs) The x86 incorporates the Sophisticated design principle once found only on mainframe and Super Computer and Servers as an excellent example (CISC)
- An alternative approach to processor design is the reduced instruction Set Computer (Risc)

The ARM architecture is used in a wide variety of embedded Systems and is one of the most powerful and best designed Risc based system in the market in this Section and the next, we provide a brief overviews of these two Systems.

C. Microprocessors and Microcontrollers.

- Microprocessor: Chips include registers an ALU and Some sort of control unit or instruction processing Logic As transistor increased.
- Micro controller: A Micro Controller is a single chip that contain the processor non-volatile memory for the program (ROM) volatile memory for input and output (RAM) a clock and I/o control unit.

The processor portion of the micro controller has a much lower silicon area than the other core microprocessor and much higher energy efficiency.

"D"

Cortex-A, Cortex-R and Cortex-M:

- The Cortex-A and Cortex-A50 are Application processor intended for mobile devices such as Smart phones and eBook Reader as well as a Consumer device such as digital TV and home getway DSL and Cable internet modems. These processor run a higher clock frequency.
- The Cortex-R is designed to support real time applications in which the timing of events needs to be controlled with repaid response to events. They can run at a fairly high clock frequency 200MHz to 800 MHz) and have very low response latency.
- Cortex-M: Series processor have been developed primarily the microcontroller domain where the need for fast highly deterministic interrupt management is coupled with the desire for extremely low gate count and lowest possible power consumption.

(Q No 4)

A. Given the memory contents of the IAS Computer shown below.

Address Contents

1. 08A 01 0FA 21 0FB
2. 08B 01 0FA 0F 08D
3. 08C 02 0FA 21 0FB

a. Show the assembly language code for the program starting at address 08A.

Ans 1. here is a simply way to understand problem:

Contents are divided up into two 5 bit instruction LH and RH

LH instruction = 0 10FA opcode = 01

Address = 0FA RH instruction = 21 0FB opcode = 21

address = 0FB

Since this is in hexadecimal form you have to convert the numbers to binary form.

(use the IAS instruction set)

LH instruction:

01 = 0000001 = LOAD M(X)

M(X) refers to the memory address location 0FA

The first 5 bits of 0BA should read - Load M (0FA)

RH instruction:

21 = 0010000 1 = STOR M(X)

M(x) refers to the memory address location of B
The second 5 bits of 08A should read STOR M(0FB)
Finally the assembly language code of 08A 010FA20FB is
LOAD M(0FA)
STOR M(0FB)

② Here is a simply way to understand this problem:
Comten are divided up into two 5 bit instruction
LHI and RHI
LHI instruction = 010FA opcode = 01
address=0FA
RHI instruction = 0F08D opcode=0F
address= 08D
Since this in hexadecimal form you have to convert the numbers to binay form.
LHI instruction:-
01=00000001 = LOAD M(X)
M(X) refers to the binar memory address location 0FA
The first 5 bits of 08B should read LOAD M(0FA)
RHI instruction:
0F=0000111 = jump+M(X10:19) refer to the memory address location 08D
The second 5 bits of 08B should Read - jump+M(08D0:18)
Finally the assembly language code for 08B and 010F08D is
LOAD M(0FA) Jump+M(08D 0:18)

(3) Here is a simply way to understand this problems:
Contents are divided up into two 5 bit instructions
LH and RH
LH instruction = 02 0FA. opcode = 02
address = 0FA RH instruction = 21 0FB
Opcode = 21 address = 0FB
Since the hexadecimal form you have to convert to the number
LH instruction:
02 = 00000010 = LOAD - M(x)
M(x) refers to the memory address location of A
The first 5 bits of 08C should read - LOAD - M(0FA)
RH instruction 21 = 00100001 = STOR M(x)
M(x) refers to the memory location 0FB
The second 5 bits of 08C should Read STOR M(0FB)
Finally the assembly language code for 08C 020FA210FB is
LOAD - M(0FA)
STOR M(0FB)

(b) Explain what this program does?

ANS: (1) In 08A address the M(0FA) transfer to the accumulator and transfer contents of accumulator to memory location 0FB

(2) In 08B address the M(0FA) transfer to the accumulator and take next instruction from left half of M(08D)

(3) In 08C address, the - M(0FA) transfer to

to contents of accumulator to memory Location OFB.

'B'

Ans. Format of machine code instructions:

- In an IAS a machine instruction will be stored with tow parts: opcode and operand the memory address 2 can be load into the accumulator as follow:

opcode : 0 0000001

operand : 00 00000010

- Two trips to memory for CPU needed to make to complete this instruction during the instruction cycle. CPU has to make accon memory to fetch the instruction which contain the address of the data we want to load

The END