NAME M.Bilal

ID 14726

Dept BS(cs)

Semester 4th

Assignment No 5

Give detail answer to each of the following:

a) Discuss different types of Semiconductor memories in detail.

Ans There are various types of Semiconductor memories. The most common is refered to as RAM (random access memory). Most types have the property of RANDOM ACCESS MEMORY which means that it takes the same amount of time to access any memory location.

Here is a table of Semiconductor Memory types.

Memory type	Category	Erasure	write mechanism	volatility
RAM (random memory)	Read/write memory	Electrically, Byte level	Electrically	volatile
ROM	Read-only memory	Not Posible	Masks	Non volatile
PROM				
EPROM		UV-light, chip level		
EEPROM		Electrically, byte level	Electri-cally	
Flash memory	Read mostly memory	Electrically, block level		

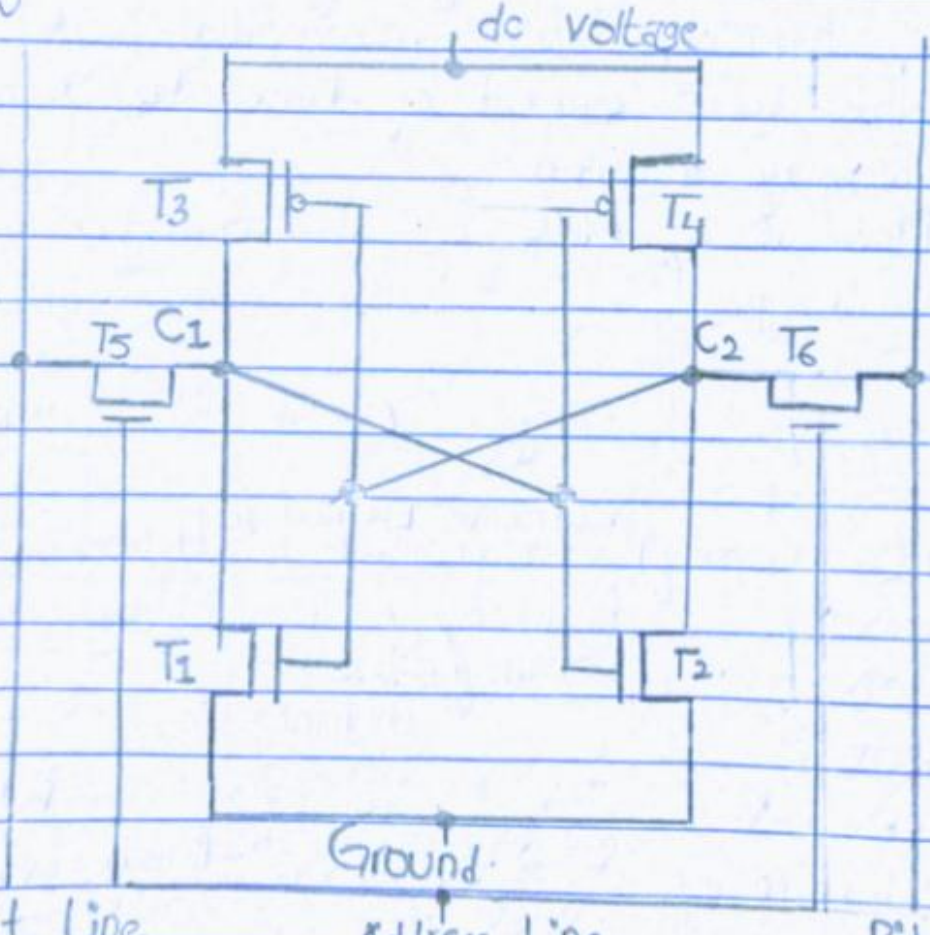
b) Explain the read and write operation for the SRAM cell using diagram.

Ans. Read operation:-

In SRAM, for any operation to be performed, the word line should be high. To perform read operation, initially....

* Write operation:-

Consider the memory bits consists of $Q = 0$ and $Q' = 1$.



(b) Static RAM (SRAM) cell

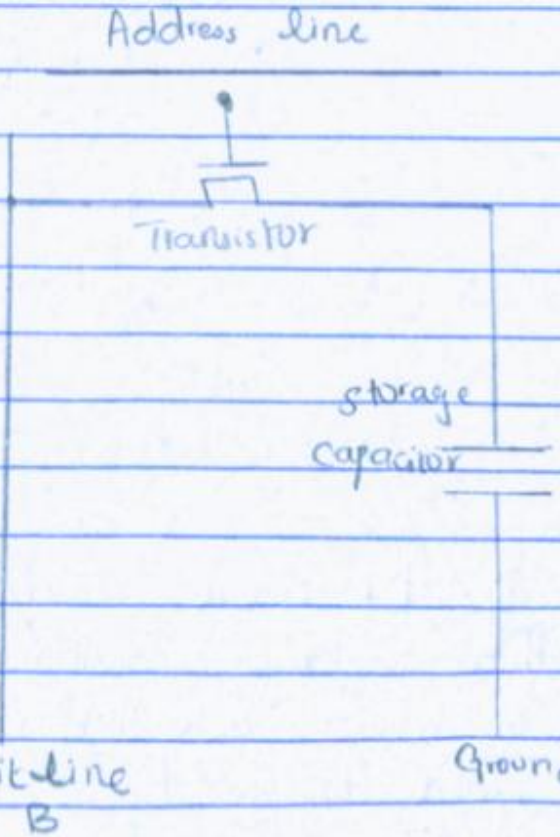
c) Explain the read and write operation for the DRAM cell using diagram.

Ans) Read operation:-

When the address line is selected, the transistor turns on and the charge stored on the capacitor is fed out onto a bit line & to a sense line amplifier. It compares the capacitor voltage to a reference value & determines if the cell contains a logic 1 or a logic 0.

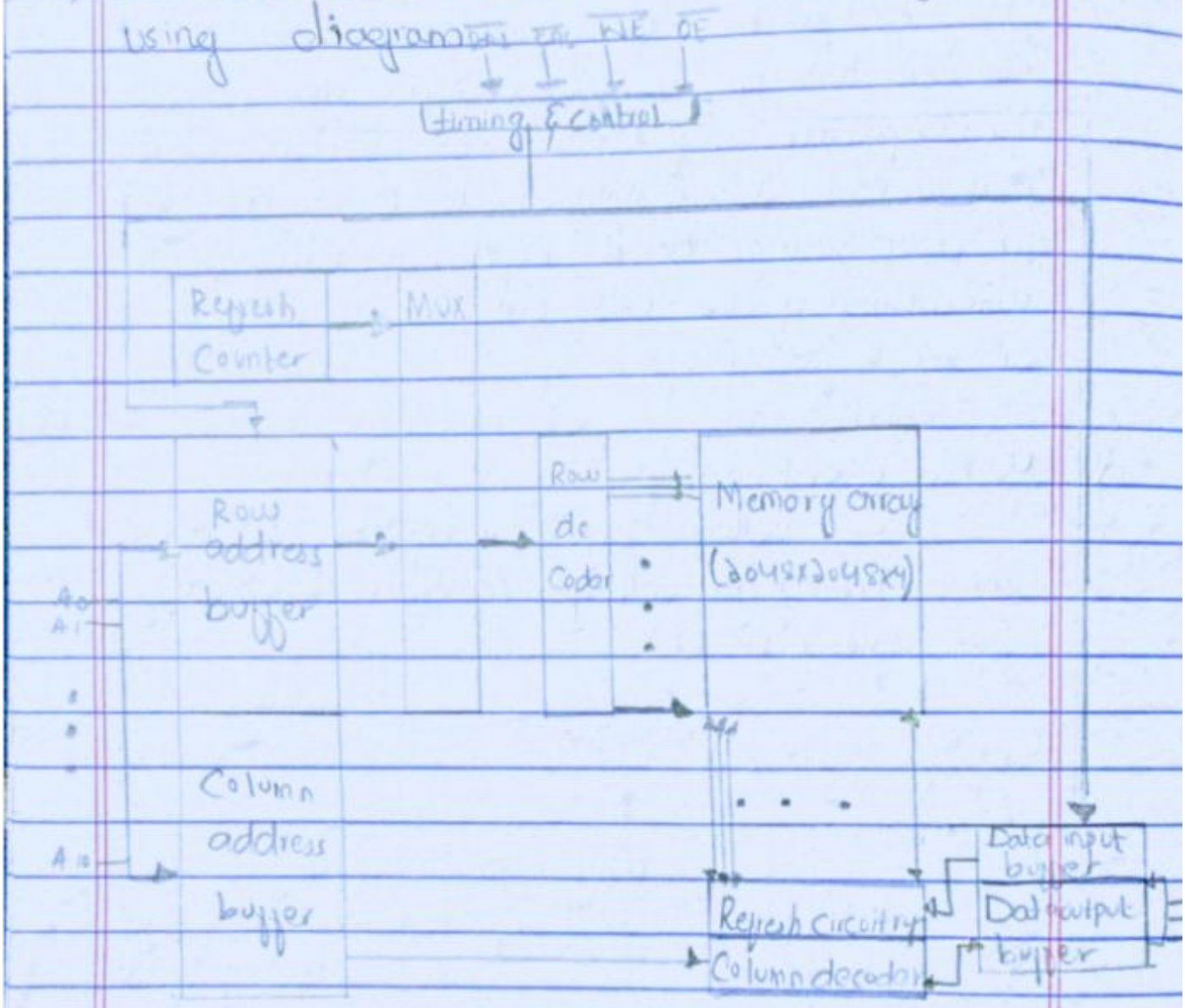
Write operation:-

A voltage signal is applied to a bit line: a high voltage represents 1 & a low represents 0.



Date: / /

d) Discuss 16-Mbit DRAM (4M×4) organization using diagram



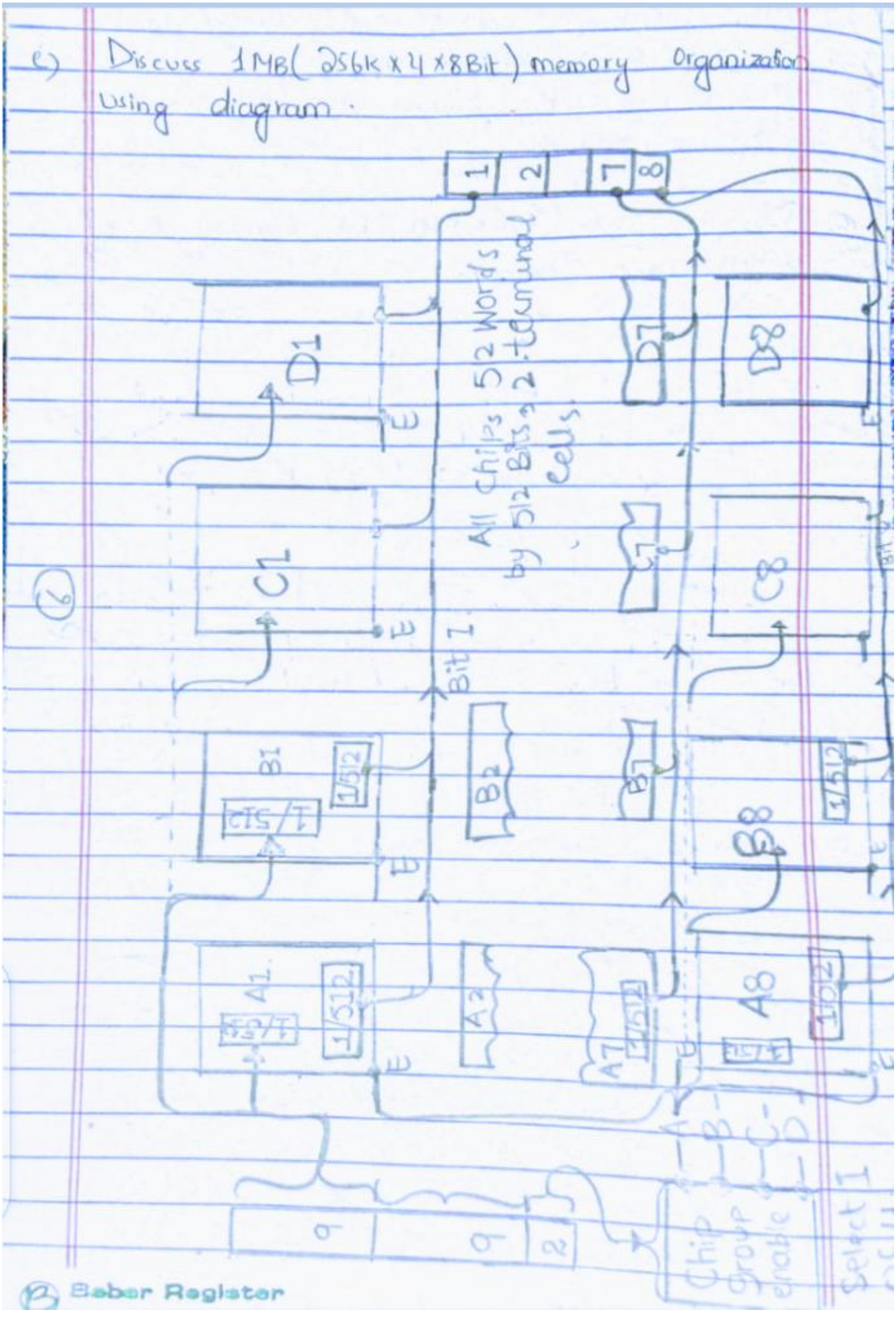
Typical 16-Mbit DRAM (4M×4)

Because only 4 bits are read/written to this DRAM, there must be multiple DRAMs connected to the memory controller to read/write a word of data to the bus.

All the DRAMs require a refresh operation. A simple technique for refreshing is, in effect, to disable the DRAM

chip while all data cells are refreshed
The refresh counter steps through all of the
row values. This causes each cell in row
to be refreshed.

c) Discuss 1MB(256K x 4 x 8Bit) memory organization using diagram.



Baber Register

SEC-DED for each 32 bits of memory, for a 22% overhead.

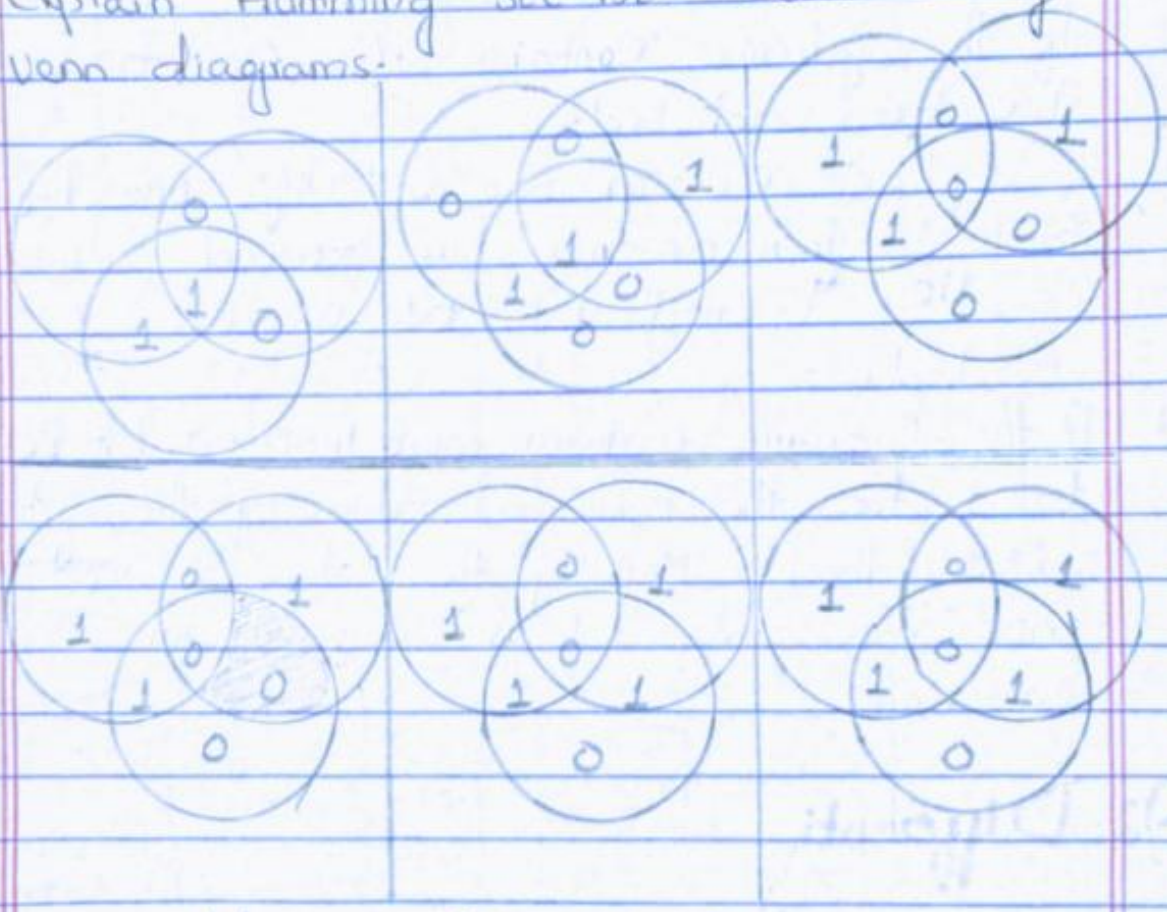
g) How is syndrome for the Haming code interpreted?

Ans Sydrome for the Hamming code interpreted as follows.

* If the Sydrome Contains all 0s, no error has been detected.
* If Sydrome Contains one and only one bit set to 1, then an error has occured in one of the 4 check bits. No Correction is needed.
* If the Sydrome contains more than one bit set to 1, then the numerical value of the Sydrome indicates the position of the data bit in error. This data bit is inverted for Correction.

The possible organization is required of a memory consisting of 1M word by 8 bits per word. In this case we have four colums of chips, each column containing 256k words arranged.

f) Explain Hamming SEC-DEC code using venn diagrams.



Hamming SEC-DEC code

With 1 bit-per-chip organization, an SEC-DEC code is generally considered adequate. e.g the IBM 30xx implementations used an 8-bit SEC-DEC code for each 64 bits of data in main memory. The size of main memory is actually about 12% larger than is apparent to the user. The VAX computers used a 7-bit

Q2 Differentiate each of the following.

a) DRAM and SRAM.

	DRAM	SRAM
*	DRAM is more dense and less expensive.	SRAM is expensive.
*	DRM requires the supporting refresh circuitry	SRAM does not require any refresh circuitry.
*	DRAM are normal in speed.	SRAM are faster in speed than DRAM.
*	SRAM is used for cache memory.	DRAM is used for main memory.

b) EEPROM and flash memory.

	EEPROM	Flash memory
*	EEPROM devices can erase any byte of memory at any time.	* Flash memory can only erase an entire chunk, or "sector" of memory at a time.
*	EEPROM uses Nor type memory.	Flash memory uses NAND type memory.
*	EEPROM is byte-wise erasable.	Flash is block-wise erasable.

c) Hard failure and Soft error in Semiconductor memories.

Ans A hard failure is a permanent physical defect so that the memory cell or cells affected cannot reliably store data but become stuck at 0 or 1 or switch erratically b/w 0 and 1. Hard errors can be caused by harsh environmental abuse, manufacturing defects, and wear.

where as

Softerror is a random, nondestructive even that alters the contents of one or more memory cells without damaging the memory. Soft errors can be caused by power supply problems or alpha particles.

Q3 Suppose an 8-bit data word stored in memory is 10101010. Using the Hamming algorithm, determine what check bits would be stored in memory with the data word. Show how you get answer.

Ans

$M = 8$

$2^k - 1 >= k + m$

$2^4 - 1 >= 4 + 8$

$15 >= 12$.

1	2	3	4	5	6	7	8	9	10	11	12
1	0	1	1	1	0	0	1	0	0	1	0

The check bits are in a bit numbers 1, 2, 4 & 8.

- Check bit 8 calculated by value in bit numbers: 9, 10, 11 and 12.
- Check bit 4 calculated by values in bit numbers: 5, 6, 7 and 12.
- Check bit 2 calculated by values in bit numbers: 3, 6, 7, 10 and 11
- Check bit 1 calculated by values in Bit numbers: 3, 5, 7, 9, 10 and 11.

Thus, the check bits are: 1011