Assignment NO: #2
Computer Architecture

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Q: Give answer to each of the following:

A/ Discuss diff develop applications that require the great Power of Contemporary microprocessor based system?

Ans/ Based system are.

- image processing
- Three dimensional rendering
- speech recognition

video confering
multimedia authoring
Voice and video annotation of files
Simulation modeling

3 Discuss the techniques used procesor to increase speed?

The technique used in contemporary processors to increase speed are following.

* Pipelining :

Pipelining inables a processor to work simultaneously on multiple instruction at the same time.

* Branch Prediction:

Branch Prediction potentially increases the amount of work available for the processor to execute.

* Speculative execution:

This enables the processor to keep its execution engines as busy as possible by executing instruction that are likely to be needed.

* Super scaler execution:

This is the ability to execute that one instruction in every processor clock cycle, in effect multiple parallel Pipelines are used.

c) Discuss the problems created due to increase in clock speed and logic density of the processor?

Ans) Discuss the problem created due to increase in clock speed and logic density of processor are.

Ans Power:

As the density of logic and the clock speed on a chip increase, so the power density increases and also dissipated the heat.

RC Delay:

The speed at which electrons can flow on a chip between transistors is limited by the resistance and capacitance of the metal wire connecting specifically, delay increases as the RC product increases.

Memory latency:

Memory access speed and transfer speed lag processor speeds.

D/ Discuss the speed up of a program using multiple processor Compared to a single Processor using Amdal's law

The speedup using a parallel processor with N processors that fully exploits the Parallel Portion of the program is as follows.

speedup = Time to exicute program on a single processor / time to execute program on N parallel Processor

$= T(1-F) + T_f / T(1-f) + T_f / N = 1/(1-F) \neq (N)$

Discuss the multicore Mic and GPGPU in detail?

The use of multiple Processor on the same chip provides the potential to increase Performance with out increasing the clock rate.

Strategy is to use two Simpler processor On the chip after rather Then One more Complex processor.

with two processor larger caches are justified.

As caches became larger it made performance sense to create two and then three levels of cache on a chip.

MIC

Leap in performance as well as the challenges in developing software to exploit such as a large number of cores.

The multiple and involves a homogeneous collection of general purpose processor on a single chip.

GPUs:

Core designed to perform parallel operation on graphics data traditionally found on a plug in graphics card. it is used to encode and render 2D and 3D graphics as well as process video.

used as vector processor for a variety of applications that require repetitive computations.

2 Solve each of the following?

A benchmark program is run on a 60 MHz processor. The execute program consists of 106,000 instruction execution with the instructions mix and clock cycle count given below. Determine ?

Instruction type	instruction count	cycle per
Integer arthemtic	46000	1
Data transfer	33000	2
Floating point	16000	2
Control transfer	9000	2

Ans.

Effective CPI:

CPI $(1 \times 46000) + (2 \times 33000) + (2 \times 16000) + 2 \times 9000 / 100$

CPI $162000/100$

CPI $= 1620$

mips Rate.

mips rate $= 60$ MHz $/ 16.20 \times 10_6$

mips rate $= 60 \times 10_6 / 1620 \times 10_6$

mips rate $= 60/1620$

Execution time.

$T = Ic / mips \times 10_6)$

$T = 104000 / 0.037 \times 10^6$

$T = 104000 / 37 \times 10_3$

$T = 2811 \times 10_3$

$T = 2.811$ Sec

B. Consider two different machines with two different instruction, both of which have a clock rate of 200 mHz.

Instruction type	Instruction count	Cycles per
Machine A	8	1
Arthematic and Pogic	4	3
Load and store	2	4
Branch, Others	4	3

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machine A

Arthematic and Pogic	10	1
Load and store	8	2
Branch	2	4
Others.	4	3

Determin the effective CPI mips and execution time for each machine.

Ans.

For machine A.

CPI = (1*8 + 3*4 + 6*2 + 3*4) * 10^6 / (8+4+2+4) * 10^6

CPI = 40 * 10^6 / 18 * 10^6

CPI = 2.22

mips rate = 200 mHz / 2.22 * 10^6

mips rate = 200 * 10^6 / 2.22 * 10^6

mips rate = 90.

mips rate = 200 mHz / 2.222 * 10^6

mips rate ∝ 200 * 10^6 / 2.22 * 10^6

T = Ic / mips * 10^6

T = 18 * 10^6 / 90 * 10^6

T = 0.2 Sec

For machine B

CPI = (1*16 + 2*8 + 4*2 + 3*4) * 10^6 / (16+8+2+4) * 10^6

CPI = 64/24

CPI = 1.92.

CPI = 1.92

mips rate = 200 mHz / 1.92 * 10^6

mips rate = 200 * 10^6 / 1.92 * 10^6

mips rate = 104

T = Ic / mips * 10^6

T = 24 * 10^6 / 104 * 10^6

T = 0.23 Sec

c) Early example of CISC and RISC design are the VAX 11/780 and the IBM RS/6000 respectively using a typical benchmark program

Processor	Clock frequency	Performance (Pi)
VAX 11/780	5	1
IBM RS/6000	25	18

Q. what are relative size of the instruction count of the machine code for this benchmark?

The mips rate could be computed as following

mips rate = IC / T × 10^6

IC mips rate = T × 10^6

Now by computing the ratio of instruction count of the IBM

18 × 1x × 10^6 / 1 × 12x 10^6

= 18 / 12

= 1.5

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b) what are CPI values for the two machines

Ans/ Regarding to the VAX 11/780 the CPI

5 MHz (1 × 10^6) = 5 × 10^6 / 1 × 10^6

= 1/1 = 5

= 25/18 = 1.4

D.

a) Determine the average CPI
b) Determine the corresponding mips rate
c) Calculate the speedup factor.)
d) Compare the actual speedup factor with o the theoretical speedup factors determine by the Amdal's law?

ans 1. Since we have the same instruction mix, that means the additional instruction for each taste could be allocated appropriately between the instruction types. Therefore the following table be

instruction-typ.	CPI	instruction Mix
Arithmetic and Pagic	1	60%.
Load	2	18%.
Branch	4	12%.
Memory reference with cache miss.	12	10%.

The average CPI = (1 x 0.6) + (2 x 0.18) + (4 x 0.12) + (12 x 0.1) = 2.64. Therefore the CPI has been increased

Since the time for memory accessed is also increased

b). mips. 400/2.64 = 152. There is a corresponding drop in the mips rate.

c) The speed up factor equals to the ration of the execution times. The execution time is calculated as following.

$$T = Ic / (mips \times 10^6)$$

For the one processor $T_1 = (2 \times 10^6)(178 \times 10^6) = 11$ ms.

For the 8 Processor each processor executes 1/8 of the 2 million plus the 25,000

$$T_8 = 2 \times 10^6 + 8 + 0.02 \times 10^6 / 152 \times 10^6$$

$$T_8 = 1.8 \text{ ms}$$

Therefore we have speed up Time to execute program on a single processor.

Time to execute Program on N Parallel processor.

speed = 11 / 1.8.

Speed up = 6.11

d) By depending to the give information given it is not obvious how to equan f y this effect in Amdal's equation. Therefore it is suposed that the fraction of code which is Parallelizable is f = 1 Then Amdal's law address to speedup = N = 8. Therefore the actual speed up is only about 75% of the theoritical speed up