Assignment NO 1
Computer Architecture

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(Q: NO: 1)

Give answers to each of the following ?

(A)

What are the main function of Computer :?

i) Data processing::
Data may take a wide variety of forms and the range of processing requirement is broad.

2) Data storage::
The computer performs a long term data storage function. Files of data are stored on the computer for subsequent retrieval and update.

3- Data movement:
When data are moved over longa distances, to or from a remote device the process is known as data Communication

4- Control:
With in Computer a Control unit manages the Computer resources and orchastrates the performance of its functional parts in response to instruction

B. Briefly explain the function of each sub-area.?

Ans: ISU:
Determines the sequence of in which instruction are executed in what is refered to as a superscalar Architecture

IFU: Logic for fetching instruction

IDU:
The IDU is feed from the IFU buffers and responsible for the parsing and decoding of all x/ architecture operation Codes

LSU: It is responsible for handling all types of operand access data

all lengths, modes and formats as defined in the z/Architecture

XU :

The unit translates logical addresses from instruction into physical addresses in main memory.

It contains TLB used to speed up memory access.

FXU : The FXU executes fixed point arithematic operation

BFU :

The BFU handles all binary and hexadecimal floating point operation as well as fixed point multiplication operation

DFU :

The DFU handles both fixed point and floating point operation on number that are stored as decimal signals

RU :

The RU keeps a copy of the complete state of the system that includes all register, collects hardware fault signals.

CoP:
The CoP is responsible for data compression and encryption function for each Core.

I- Cache:
This is 64- KB L1 instruction Cache allowing the IFU to prefetch instruction before they are needed

L2 Control:
This is the control logic that manages the traffic through the two L2 Caches

Instr L2
A 1-MB L2 instruction Cache

Data L2.
A 1-MB data Cache for all memory traffic other than

C.
Discuss the IAS operation using flow chart in fig 02.

And The IAS operates by Repeatedly Performing an instruction cycle. each instruction cycle consists of two sub cycles

Fetch cycle:

The opcode of next instruction is loaded into the IR and the adress portion is loaded into the MAR. This instruction may be taken from the IBR, Or it can be obtained from memory by loading a word into the MBR and then down the IBR and MAR and IR

Execute Cycle:

The Control Circuitry interprets the opcode & executes the instruction by sending out the loaded out the appropriate Control Signal to cause data to be moved or an operation to be performed by the ALU

D- For each of the following examples, determine wheather this is an embedded system, explaining why or why not.

2. Are programs that understand Physics and hardware embedded?

e.g one that uses finite element methods to predict fluid flows over airplane wings?

Ans: No. The Programs are never considered to be embedded because they are not an integral component of a larger system.

b) Is the internal microprocessor controlling a disk drive an example of an embedded system?

Regardless of the disk drive is set for. The software within the disk drive control the HDD hardware and is hard real time as well.

c) I/O drivers control hardware, so does the presence of an I/O driver imply that the computer executing the driver is embedded?

No. input, output drivers do not represent the embedded system.

d. is a PDA an embedded system?

Yes PDA is embedded system because it is just like a personal

e) Is the microprocessor controlling a cell phone an embedded system

Ans) Yes the firmware in the cell phone is controlling the radio hardware.

f) Are the computer in big phased-array radar considered embedded. These radars are 10-story building with one to three 100-foot diameter radiating patches on the slopped sides of the building?

Ans) Yes, these computer were formerly some of the most powerful available when the system was built are located in large computer room occupying almost one whole floor of a building and may be hundreds of miles away from the radar hardware. However the software running in the computer controls the radar hardware therefore the computer are an integral component of a larger system.

g) Is a traditional flight management system (FMS) built into an airplane cockpit considered embedded?
If the FMS is not connected to the avionics and is used only for logistics computerizations a function usually performed on a laptop then the FMS already not embedded.

h) Are the computer in a hardware in the loop (HIL) simulator embedded?
Yes, both in the simulator and in the thing being tested in the HIL simulator. Hardware is being controlled on both sides.

i) Is the computer controlling a pacemaker in a person's chest an embedded computer?
Yes in this case of the system is the combination of the pacemaker and the person's heart

i) Is the computer controlling fuel injection in an automobile engine embedded?
Yes it is part of large system the engine and it is directly monitoring and controlling the engine through special hardware.

Q. No: 2. Write a note on each of the following:?

A) main structural components of a Computer?

i) There are four main S components

CPU:
Controls the operation of the computer and performs its data processing functions; often simply referred to as a processor

Main memory.
Stores Data

I/O: Moves data b/w the computer and its external environment

4- System interconnections:
Some mechanism that provides for communication among CPU, main memory and I/O

8 Key characteristics of of planned Compiler family.

ns/ is follow.

- Smaller or identical instruction set.
  In some cases, the lowest end of the family has an instruction set that is subset of that of the top end of the family, this means that programs can move up that but not down.

* Similar:
  The same basic operating system is available for all family members.

* Increasing speed.
  The rate instruction execution increases in going from lowes to higher family members.

* increasing number I/O ports.
  The number of I/O ports increases in going from lower to higher family members.

* Increasing memory size:
  The size of main memory increases is going from lower to higher family members.

Increasing Cost:
At a given point in time, the cost of a system increases is going from lower to higher family members.

C/ Stored Program Computer:
A fundamental design approach first implemented in the IAS Computer is known as the stored Program Concept. The idea is usually attributed to the mathematician John von Neumann.
The first publication of the idea was in a 1945 Proposal by von Neumann for a new Computer the EDVAC. In 1946, Von Neumann and his colleagues began the design of a new stored Program Computer, referred to as the IAS Computer at the Princeton institute for advanced Studies.
It Consists of
A main memory which stores both data and instruction
An ALU capable of operating On binary data.

D/ Moore's law

The famous Moor's law which was propounded by Gordon more transistor of intel in 1995, Moore observed that the number of transistor that could be put on a single chip was doubling every year.

The Conequenas of Moore's law are profound.

1. The Cost of Comuter logic and memory Circuitry has a fallen at dramatic rate.
2. ~~Because logic~~ and dramatic rate. The cost of computer logic and memory Circuitary has fallen at a dramatic rate.
3. The Computer becomes smaller making it more convenient to place in a variety of environment
4. There is a reduction in power requirments.
5. With more Circuitary on each chip. there are fewer inter chip connection.

Q:3 Differentiate each of the following?

A) A computer organization and Computer architecture?

Computer architecture refers to those attributes of a system visible to a programmer or, put another way, those attributes that have a direct impact on the logical execution of a Program. A term that is often used interchangeably with Computer architecture is instruction set architecture.

* Computer Organization:

Refers to the operational units and their interconection that realize the architecture specification. example of architectural attributes include the instruction set the number of bits, used to represent various data types. e.g / number characters I/O mechanism and techniques for addressing memory.

B/ Risc and CSc

~~Risc~~ : Cisc.

The current x86 offerings represent the results of decades design effort on Cisc. The x86 incorporates the sophisticated design principle once found only on mainframes and Supercomputer and serves as an excellent example of Cisc design.

Risc :

The ARM architecture is used a wide variety of embedded system and is one of the most Powerful and best designed Risc - based system on the market. In this section and the next we provide a brief Overview of these two systems.

c/ Micro processor and Micro Controler:-

Microprocessor :-

This chips include register, an ALU and some sort of control unit or instruction processing Logic. A transistor density increased it became possible to increase the complexity of the instruction set architecture and ultimately to add memory and more then one processor.

* A micro Controller :-

It is a single chip that Contains the processor non-volatile memory for the Program (ROM) volatile memory of input and output a clock and an I/O control unit. The Processor Portion of the micro controler has a much lower Silicon area than onth microprocessor and much higher energy efficiency.

D) Cortex-A Cortex-R and Cortex-M

The Cortex-A and Cortex-A50 are application processors intended for mobile devices such as smartphones and e-book readers as well as consumer devices such as digital TV and home gateways. These processors run at a higher clock frequency and support a memory management Unit (MMU)

Cortex-R

This is designed to support real time applications in which the timing events needs to be controlled with rapid response to events. They can run at a fairly high clock frequency and have very low response latency.

Cortex M. Series processors have been developed primarily for the microcontroller domain where the need for fast.

highly deterministic interrupt management is coupled with the desire for extremely low gate count and lowest possible Power Concumption.

Q:4 Give Solution of the cache?

Address Contents

1- 08A 010FA210FB

2- 08B 010F A0F0B1D

3:- 08C 02aFA210FB

Q Show the assembly language code for the Program starting at adress 08A.

Ans. 1- Here is a simple way to understand this Problem.

Contents are divided up into two 5 bit instruction LH and RH.

LH instruction = 010FA

opcode = 01

address = 0FA

RH instruction = 210FB

opcode = 21

address = 0FB.

Since this is in hexadecimal form you have to convert the number to binary form.

LH instruction

01 = 00000001 = LOAd (m(x)

m(x) refers to the memory adress location 0FA

The first 5 bits of 08A should read LOAD(m(0FA)

The second 5 bits

RH instruction 00100001=StoRm(x)

m(x) refer to the memory adress location 0F13.

Finally the assembly language code for 08A 010FA 210FB is

LOAD m(0FA)

StoR (m(0FB)

Here is a simple way to understand this Problems.

Contents are divided up into two 5 bit instruction LH and RH

LH instruction = 010FA

opcode = 01

adress = 0FA.

RH instruction = 0F08D
opcode = 0F
adress = 08D
Since this is an hexadecimal from from you have to convert the number to binary form.

LH instruction
01 = 00000001 = LOAD M(x).
M(x) refer the memory adress location 0FA
The first 5 bits of 08B should read LOAD. M(0FA)

RH instruction
0F = 00001111 = Jump+M(x,0:19) refers to the memory adress location 08D
The second 5 bit of 08B Should read - Jump +(M08D,0:19)
Finally the assembly language code for 08B 01 0FA 0F 08D is
LOAD M(0FA)
Jump + (M(08D, 0:19)
Here is simple way to understand this Problem
Contents are divided up into two 5

5 bits LH and RH.

LH instruction 02CFA.

opcode : 21

adress OFB.

Since this hexadecimal from you have to convert the number to binary form. LH instruction.

$02 = 0000001_2$ = LOAD - M(x)

m(x) refers to the memory adress location OFA.

The first 5 bits of osc should read - STOR M(OFB)

Finally the assembly language code for osc 02CFA210FB is

LOAD m(OFA)

STORm(OFB)

b) Explain what this Program does?

- In osc adress transfer to the accumulator and transfer contents of accumulator to memory location OFB.

In osc adress - M(OFA) transfer to the accumulator and transfer contents of accumulator to memory location OFB.

END...