

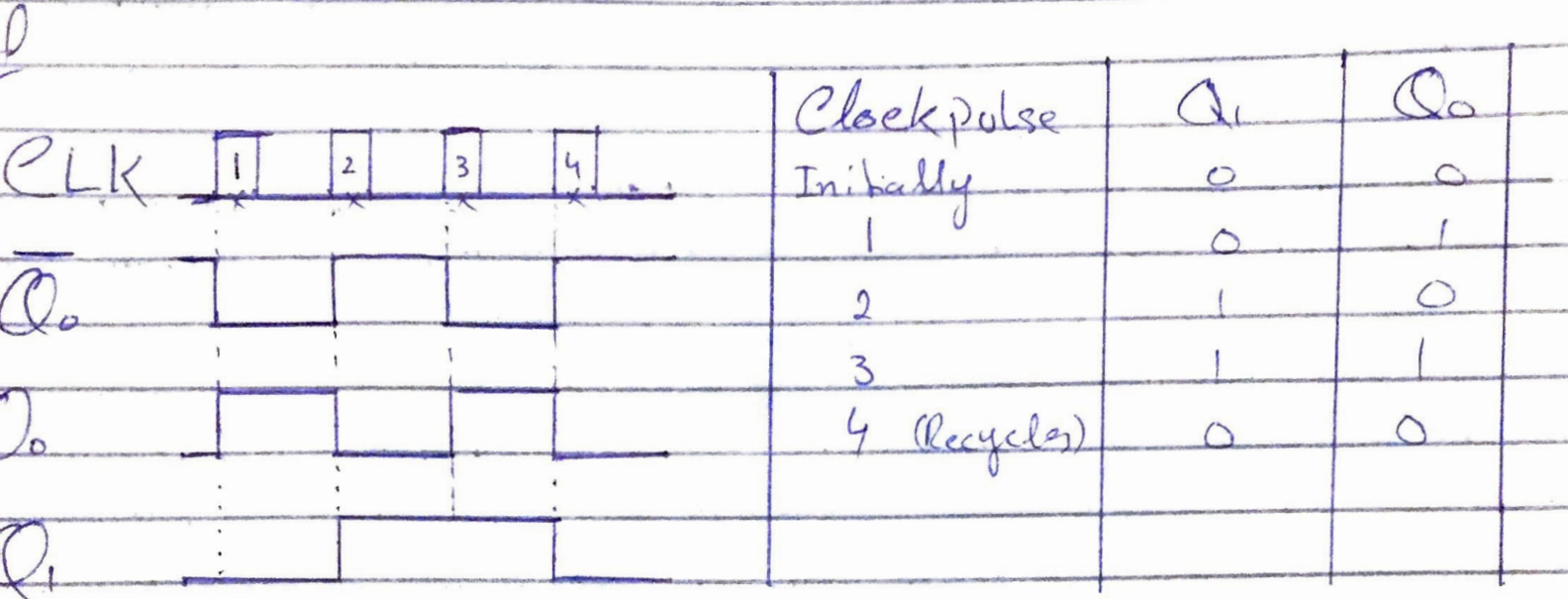
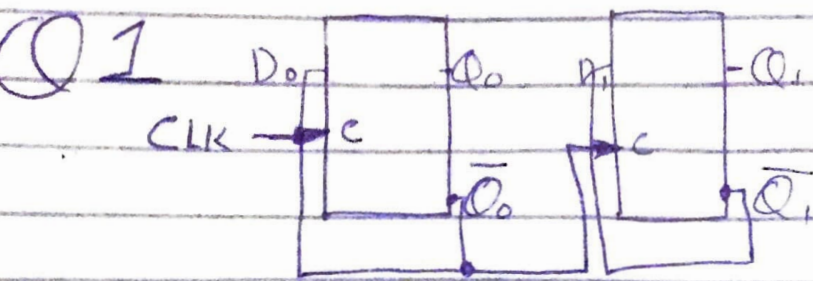
Digital Logic Design

Assignment 8
Sir. Muhammad Amin

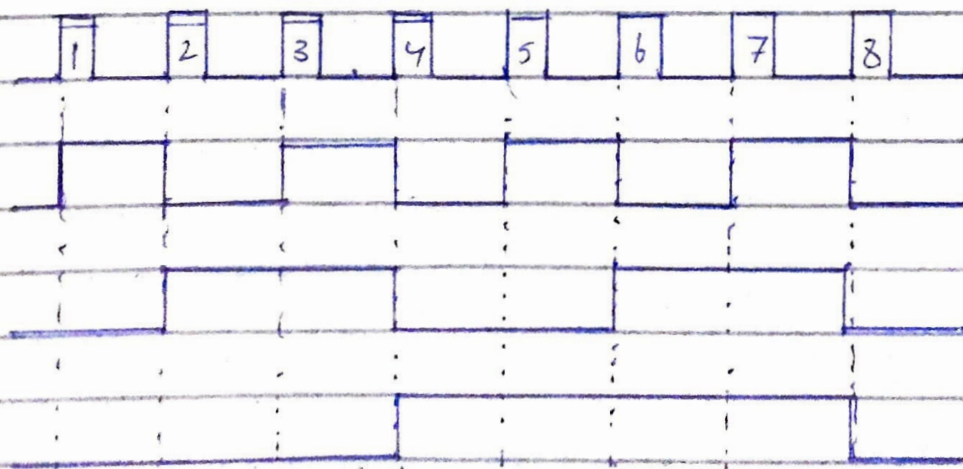
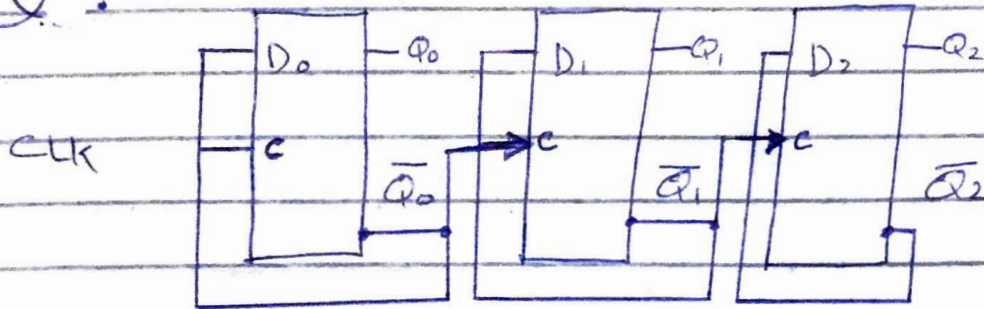


HASSAN MEHDI

15453
Csc-201



Q : 2



C. Pulse	Q2	Q1	Q0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (Recycle)	0	0	0

Q 3

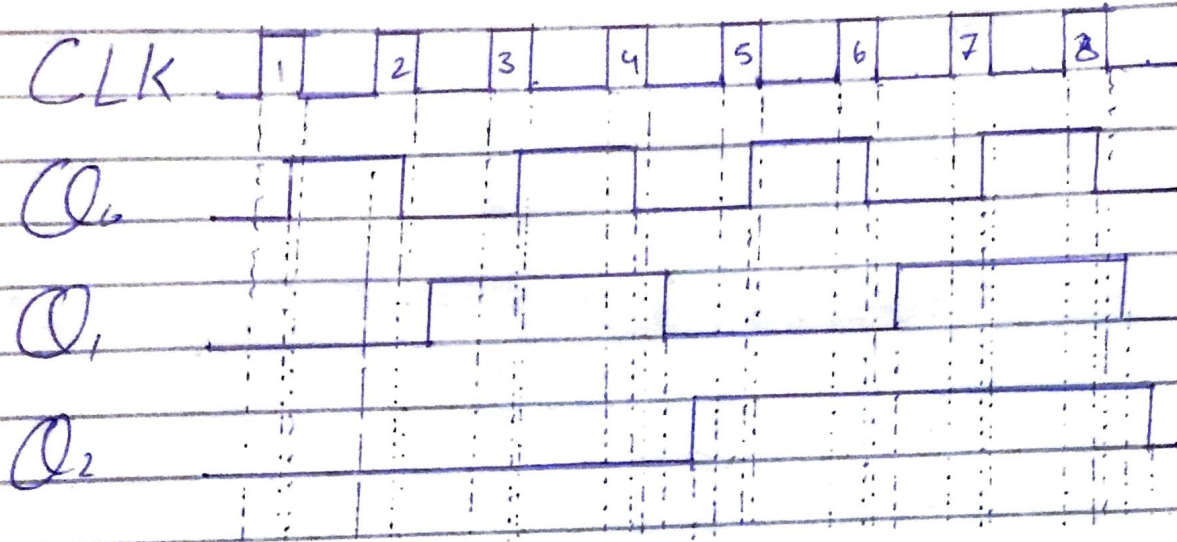


The worst case delay occurs on
CLK - Q₀,

The highest delay is 8ns, because in the case of synchronous binary counters, the propagation delay is independent of the number of flip-flops used.

Q9

Asynchronous

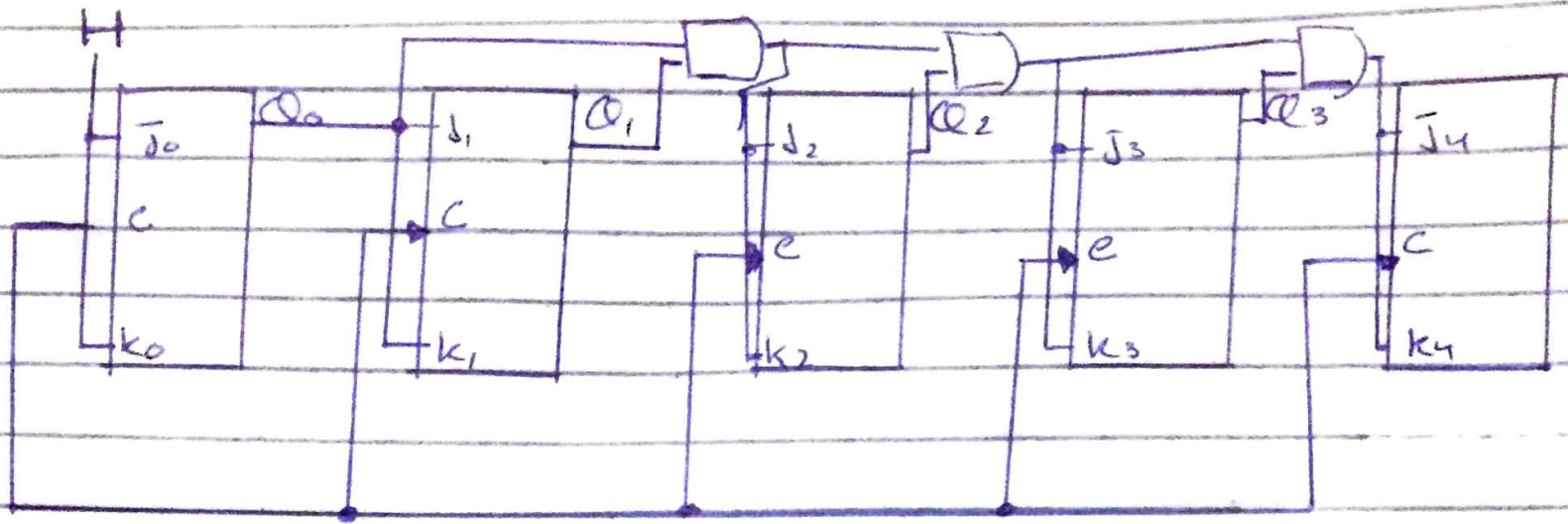


The worst case delay time occurs at Q₂.

The delay interval equals to three times of the delay time at Q₂.

$$3(8ns) = 24ns$$

Q5



CLK	1	2	3	4	5	6	7	8
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Q0	0	0	0	0	0	0	0	0
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Q1	0	0	0	0	0	0	0	0
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Q2	0	0	0	0	0	0	0	0
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Q3	0	0	0	0	0	0	0	0
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Q4	0	0	0	0	0	0	0	0
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C. pulse	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄
Initially	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1
18	1	0	0	1	0
19	1	0	0	1	1
20	1	0	1	0	0
21	1	0	1	0	1
22	1	0	1	1	0
23	1	0	1	1	1
24	1	1	0	0	0
25	1	1	0	0	1
26	1	1	0	1	0
27	1	1	0	1	1
28	1	1	1	0	0
29	1	1	1	0	1
30	1	1	1	1	0
31	1	1	1	1	1