Assignment: 1

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Q.1

Ans: A

1) Data processing: Data may take a wide variety of forms, and the range of processing requirements is broad.

2) Data storage: Even if the computer is processing data on the fly (i.e., data come in and get processed, and the results go out immediately), the computer must temporarily store at least those pieces of data that are being worked on at any given moment

3) Data movement: The computer's operating environment consists of devices that serve as either sources or destinations of data. When data are received from or delivered to a device that is directly connected to the computer.

4) Control: Within the computer, a control unit manages the computer's resources and orchestrates the performance of its functional parts in response to instructions.

Ans: B

1) ISU (instruction sequence unit): Determines the sequence in which instructions are executed in what is referred to as a superscalar architecture.
2) IFU (instruction fech unit): Logic for fetching instruction.

3) IDU (instruction decode unit): The IDU is fed from the IFU buffers, and is responsible for the parsing and decoding of all z/Architecture operation codes.

4) LSU (load-store unit): The load contains the 96-KB L1 data cache 1, and manages data traffic between the L2 data cache and the functional execution units.
5) XU (translation unit): This unit translates logical addresses from instructions into physical addresses in main memory.
6) BFU (Binary floating-point unit): The BFU handles all binary and hexadecimal floating-point operations, as well as fixed-point multiplication operations.

7) DFU (decimal floating-point unit): The DFU handles both fixed-point

and floating-point operations on numbers that are stored as decimal digits

8) RU (recovery unit): The RU keeps a copy of the complete state of the system that includes all registers, collects hardware fault signal, and manages the hardware recovery actions.

9) COP (dedicated coprocessor): The COP is responsible for data compression and encryption function for each core.

10) I-Cache: This is 64-KB L_1 instruction cache, allowing the IFU to prefect instruction before they are needed.

11) L2 Control: This is the control logic that manages the traffic through the two L2 caches.

12) Data-L2: A 1-MB L_2 data cache for all memory traffic other than instructions

13) Instr. L2: A 1-MB instruction cache.

Ans: C

The IAS operates by repetitively performing an instruction cycle, ~~as shown in~~ figure 2. Each instruction cycle consists of two subcycles. During the fetch cycle the opcode of the next instruction is loaded into the IR and the address portion is loaded into the MAR. This instruction may be taken from the IBR, or it can be obtained from memory by loading a word into the MBR, and then down to the IBR, IR, and MAR.

Ans: D

a. No. These programs are never considered to be embedded because they are not an integral component of a larger system.

b. yes, regardless of what the disk drive is used for. The software (firmware, actually) within the disk drive controls the HDA (head disk assembly) hardware and is hard realtime as well.

c. yes. the firmware in the cell phone is controlling the radio hardware.

f. yes, these Computers were generally so me of the most powerful Computers available when the system was built, are located in a larg Computer room occupying almost one whole floor of a building and may be hundreds of meters away from the rader hardware. However the software running in these Computer controls the radar hardware. therefore, the computers are an integral component of a large system.

g: if the FMS is not connected to the avionics and is used only for logisties computerizations, a function readily performed on a laptop, then the FMS is clearly not embedded.

h: yes both in the simulator, and in the thing being tested in the HIL simulator. Hardware is being controlled on both sides.

i: yes, in this case of the "system" is the combination of the pacemaker and the person's heart.

J: yes, it is part of a large system, the engine, and it is directly monitoring and

Controlling the engine through hardware.

Q.2 Write a note on each of the following.

Ans: A There are four main structural components:

1 Central Processing Unit (CPU): Controls the operation of the computer and performs its data processing functions; often simply referred to as processor.

2- Main memory: Stores data.

3: I/O: Moves data between the computer and its external environment.

4: System interconnection: Some mechanism that provides for communication among CPU, main memory, and I/O. A common example of system interconnection is by mean of a system bus. Consisting of a number of conducting wires to which all the other components attach.

B Ans:

The characteristics of a family are as follows:

1. Similar or identical instruction set.
In many cases, the exact same set of machine instruction is supported on all members of the family. Thus, a program that executes on one machine will also execute on any other.

2: Similar or identical operating system: The same basic operating system is available for all family members.

3: Increasing speed: The rate of instruction execution increases in going from lower to higher family members.

4: Increasing memory size: The size of main memory increases in going from lower to higher family members.

5: Increasing cost: At a given point in time, the cost of a system increases in going from lower to higher family members.

Ans: C)

Stored Program computer:

1) A main memory, which stores both data and instruction.
2) An arithmetic and logic unit (ALU) capable of operating on binary data

3) A control unit, which interprets the instructions in memory and causes them to be executed

~~4) Input-ou~~

Ans: D):

Moore's Law: Moore's law refers to moores perception that the number of transistors on a microchip doubles every two years, though the cost of computers is halved. Moore's Law states that we can expect the speed and capability of our computers to increase every couple of years, and we will pay less for them.

Q.3: Differentiate each of the following:

Ans: A)

Computer architecture: refers to those attributes of a system visible a progr- ammer or, Put another way, those attri- butes that have a direct impact on the logical execution of a program. A term that is often used interchangeably with computer architecture ~~in~~ is instruction- set architeture (ISA).

Computer organization: refers to the ope- rational units and their interconnection that realize the architectural specifi- cations. Examples of architectural attr- ributes include the instruction set, the number of bits used to represent various data types (e.g., numbers, characters), I/O mechanisms, and techniques for address- ing memory. Organizational attributes in- clude those hardware details transpa- rent to the programmer.

Ans: B)

1. RISC stands for Reduced instruction set Computer.
2. RISC processors have simple instruction taking about one Clock cycle. The average Clock cycle Per instruction (CPI) is
3: Performance is optimized with more focus on software
4: It has no memory unit and uses separate hardware to implement instructions.
5; it has a hard-wired unit of programming.

CISC: 1: CISC stands for Complex instruction set Computer.
2: CISC Processor has Complex instructions that take up multiple clocks for execution.
3: Performance is optimized with more focus on hardware
4: It has a memory unit to implement complex instructions.

5: it has a microprogramming unit.

Q.4 Solve each of the following

Ans: A

a.

Address	Contents
08A	LOAD M(0FA)
	STOR M(0FB)
08B	LOAD M(0FA)
	JUMP +M(08D)
08C	LOAD -M(0FA)
08D	

b. This program is to store the absolute value of content at memory location 0FA into memory 0FB.

Ans: B

OPcode	Operand
00000001	000000000010

In the beginning the CPU have to fetch the instruction from the memory. Then the instruction will include the address of the data which is required to load. Through the execution time, the memory will be accessed in that time to load the data contents which is located at that address For a total of two trips to memory.

Ans: C

Memory Butter Register (MBR): In IAS structure a word is of length 40 bits. MBR contains a word to be stored in memory. So, the overall data paths to/from MBR are 40 bits.