Basic Electronics
BS-SE (13)

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Question 1:
Answer:

a) Formula for Zener current is :

Iz = Vs - Vz/Rs

Substitute: 24V for Vs
15V for Vz
470 ohm for Rs

Iz = 24-15/470
=>19.14 mA

Therefore the zener current is Iz = 19.14 mA

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b) The zener diode is disconnected so the circuit consists of power supply of 24 V and 2 resistors 470 ohm and 1.5 ohm in series

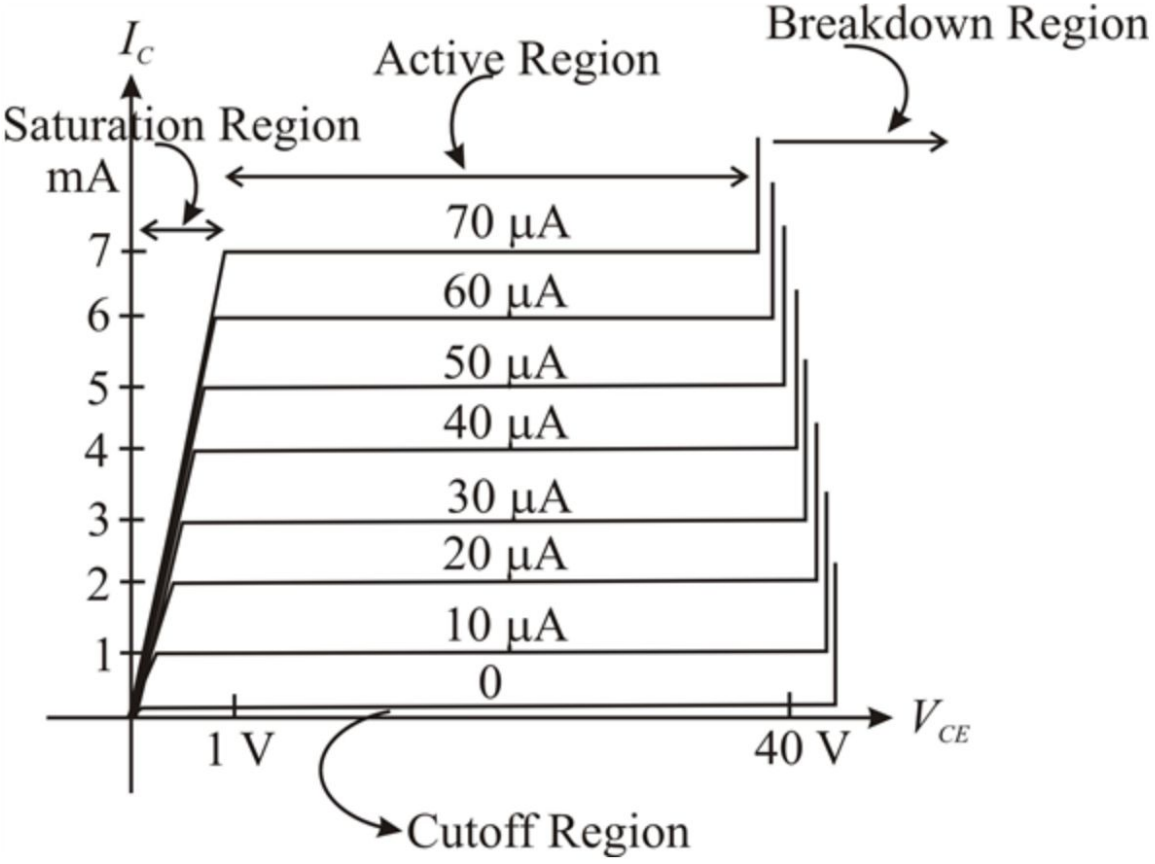
So applying the voltage division principle and calculating the load voltage

$V_L = V_s$ (1.5 k ohm / 470 ohm + 1.5 k ohm)

=> Substitute 24 V for Vs
=> V_L = 24 V (1.5 kOhm / 470 ohm + 1.5 k ohm)
=> (24 V)(0.7614)
=> 18.27 V

The load voltage is V_L= 18.27V

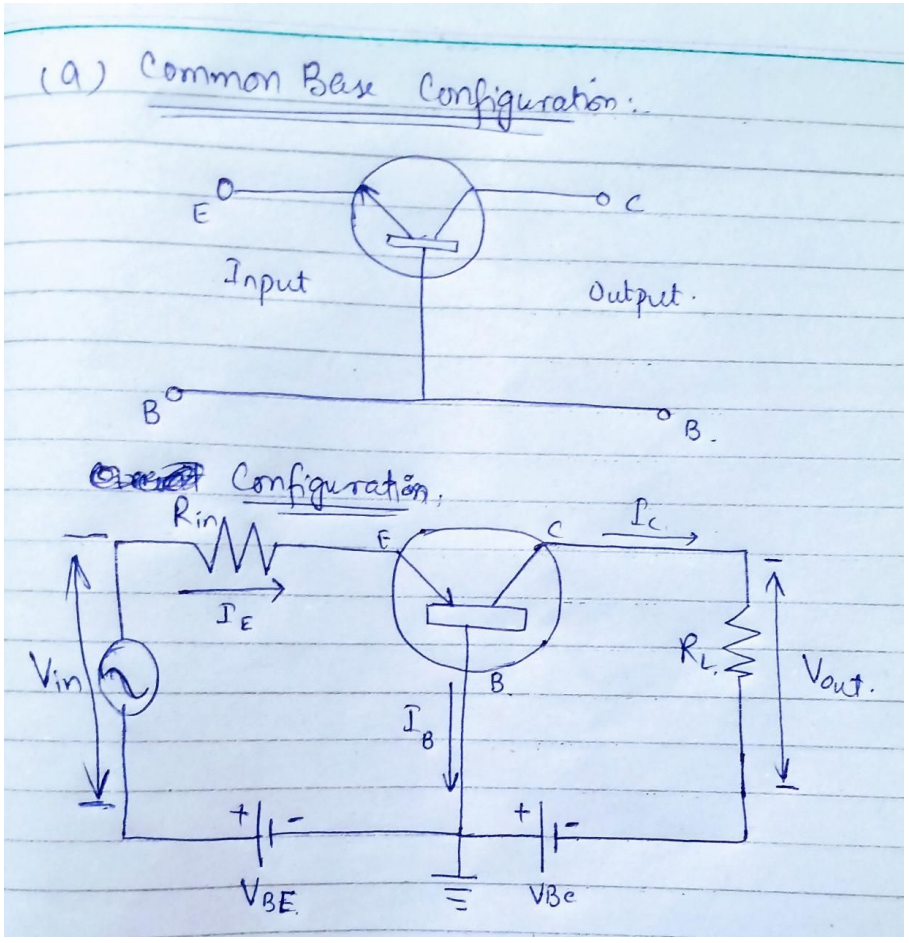
Question 2:
Answer:



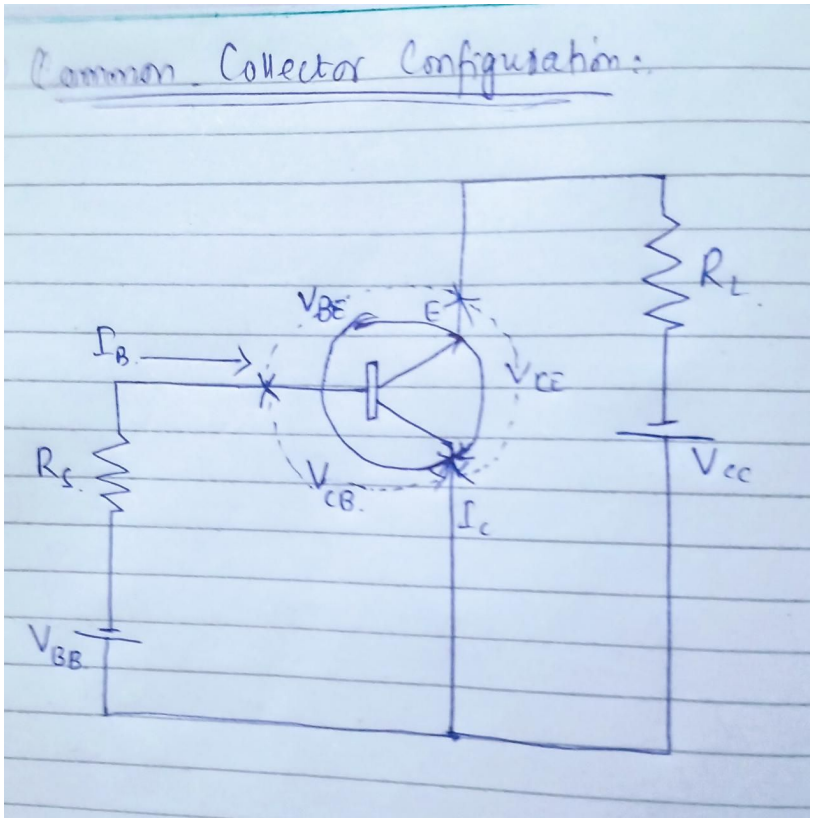
- The curves of the diagrams have different regions where the action of the transistor changes.
- The region in the middle where V_{CE} is between 1V and 40V represents the normal operation of the transistor. In this region the emitter diode is forward biased and the collector diode is reverse biased.
- Furthermore the collector is gethereing almost all the electrons that the emitter sent into the base. This is why changes in the collector voltage have no effect on the collector current. The region is called active region
- The early rising part of the curve where V_{CE} is between 0 V and a few tenths of a volt. The sloping part of the curve is called saturation region. In this region the collector diode has insufficient positive voltage to collect all the free electrons injected into the base
- The diagram has an unexpected curve, the one on the bottom. This represents the fourth possible region of operation. The base current is zero but still there is a small collector current. This bottom curve is call cutoff region of the transistor and the small collector current is called the collector cutoff current.

Question 3:
Answer:

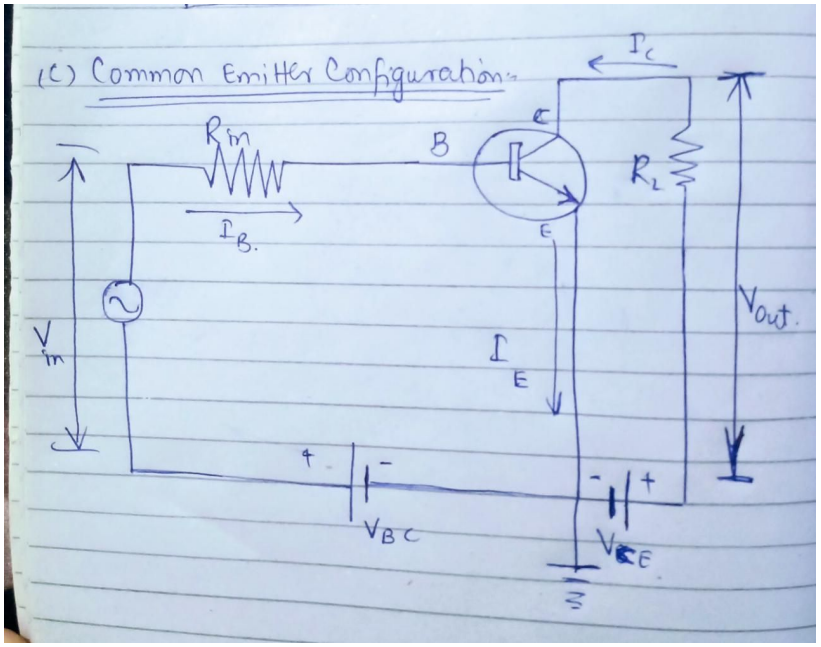
1. **Common base:** In this configuration we use base as a common terminal for both input and output signals. The configuration name itself indicates the common terminal. Here the input is applied between the base and emitter terminals and the corresponding output signal is taken between the base and collector terminals with the base terminal grounded. Here the input parameters are VEB and IE and the output parameters are VCB and IC. The input current flowing into the emitter terminal must be higher than the base current and collector current to operate the transistor, therefore the output collector current is less than the input emitter current.
   The current gain is generally equal or less than to unity for this type of configuration. The input and output signals are in-phase in this configuration. The amplifier circuit configuration of this type is called a non-inverting amplifier circuit. The construction of this configuration circuit is difficult because this type has high voltage gain values. The voltage gain for this configuration of circuit is given below.



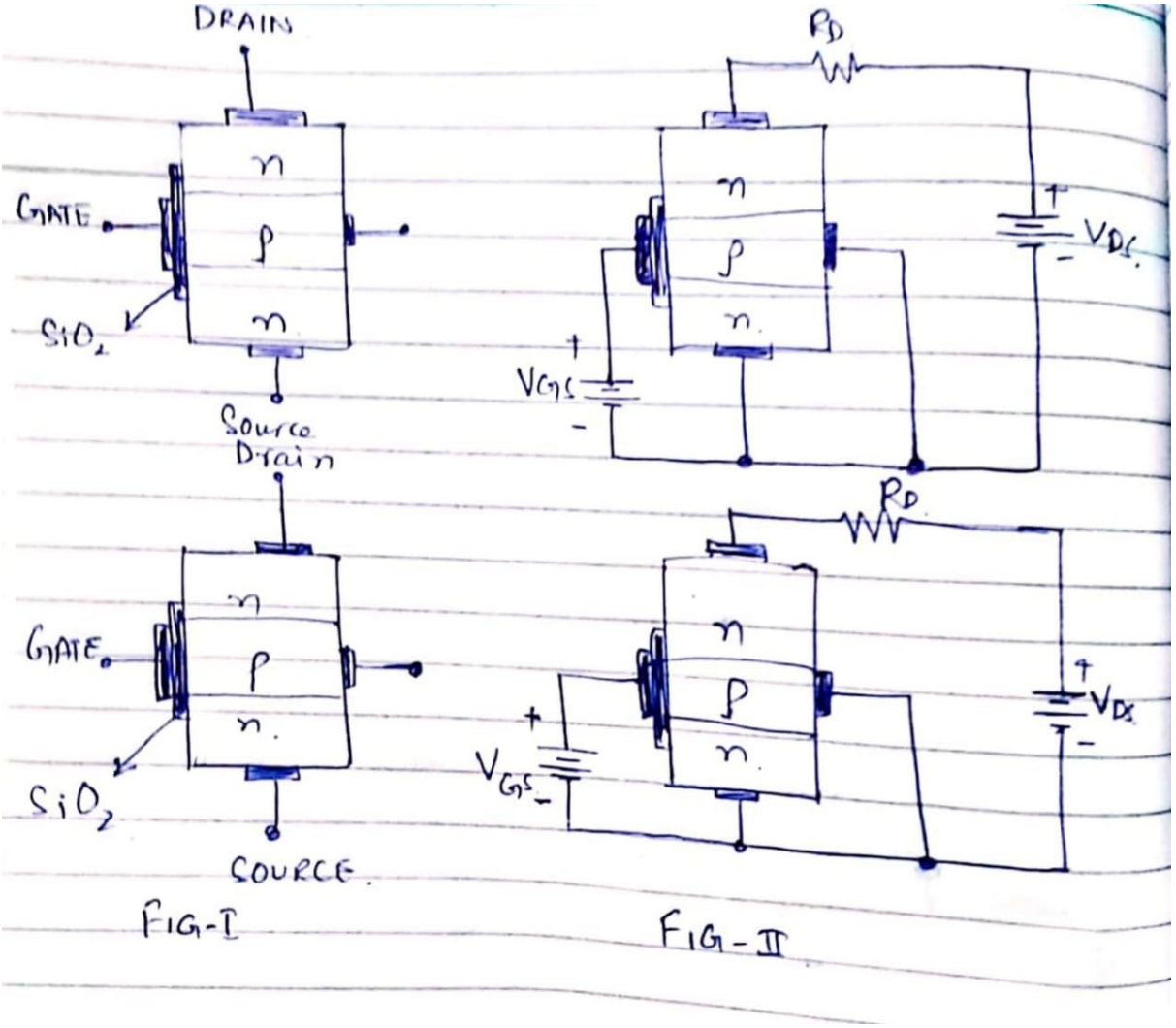
2. **Common collector:** In this configuration we use a collector terminal as common for both input and output signals. This configuration is also known as emitter follower configuration because the emitter voltage follows the base voltage. This configuration is mostly used as a buffer. These configurations are widely used in impedance matching applications because of their high input impedance. In this configuration the input signal is applied between the base-collector region and the output is taken from the emitter-collector region. Here the input parameters are VBC and IB and the output parameters are VEC and IE. The common collector configuration has high input impedance and low output impedance. The input and output signals are in phase. Here also the emitter current is equal to the sum of collector current and the base current. Now let us calculate the current gain for this configuration.



3. **Common Emitter** Configuration In this configuration we use the emitter as a common terminal for both input and output. This common emitter configuration is an inverting amplifier circuit. Here the input is applied between the base-emitter region and the output is taken between collector and emitter terminals. In this configuration the input parameters are VBE and IB and the output parameters are VCE and IC. This type of configuration is mostly used in the applications of transistor based amplifiers. In this configuration the emitter current is equal to the sum of small base current and the large collector current. i.e. IE = IC + IB. We know that the ratio between collector current and emitter current gives current gain alpha in Common Base configuration similarly the ratio between collector current and base current gives the current gain beta in common emitter configuration.



Question 4:
Answer:



- When the gate voltage is zero the current between source and drain is zero. For this reason the E-MOSFET is normally off where the gate voltage is zero.
- When the gate voltage is positive, it attracts free electrons into the p region. The free electrons recombine with the the holes next tot the silicon dioxide.
- When the gate voltage is positive enough all the holes touching the silicon dioxide are filled and free electrons begin to flow flows the source n type material next to the silicon dioxide.
- This thin conducting layer is called the n type inversion layer. When this layer is formed free electrons flow easily from source to the drain.
- The Minimum V_{GS} that creates the n type inversion layer is called the threshold voltage. $V_{GS(Th)}$.

- When V_{GS} is less than $V_{GS(Th)}$ then the drain current is zero. When $V_{GS(Th)}$ is greater than $V_{GS(Th)}$ then an n type inversion layer connects the source to the drain through which the durian current flows.

Question 5:
Answer:

a)

- The bipolar junction transistors may be destroyed by thermal runaway. The problem with the BJT is the negative temp. coefficient of V_{BE}.
- When the internal temp increases V_{BE} decrease. This increases the collector current forcing the temperature higher.
- But a higher temp reduces the VBE even more. If not properly heated, the bipolar transistor will go into thermal runaway and be destroyed.
- The disadvantage of the BJT is that it will suffer from thermal runaway at high temperatures.
- BJT cannot be connected in parallel because the VBE drops do not match closely enough.
- if you try to connect them parallel current hogging occurs this means that the transistor with the lower VBE take more collector current than the other
- Power FETs tries to hog current, its internal temp will increase,
- This increases RDS which reduces its drain current. The overall effect is for all the power FETs to give equal drain currents.
- The minority carriers of bipolar transistors are stored in the junction area during forward bias. When you try to switch off a bipolar transistor the stored charges flow for a while, Preventing a fast turnoff.
- Since a power FET does not have minority carriers it can switch a large current off faster than a bipolar transistor can.

Question 5:
Answer:

b):

- The EMOSFET is a high power application called power FET. The ser of drain curves for an n channel MOSFET. Normally EMOSFET is an OFF device.
- The minimum voltage V_{GS} that creates the n type inversion layer is called threshold voltage $V_{GS(Th)}$. When V_{GS} is less than $V_{GS(Th)}$ the drain current is approximately zero .
- When V_{GS} is greater the $V_{GS(Th)}$ the curve appears linear and the device begins to conduct and turns ON also the drain current is controlled by the gate voltage.
- Almost vertical part of the graph is the ohmic region
- Horizontal parts are the active regions
- when biased in the vertical region, EMOSFET is equivalent to a resistor.
- When biased is in the active region it is equivalent to a current source.
- In the cutoff region the gate source voltage is less than the gate threshold voltage and the device is an open circuit or OFF.
- Drain current is a function of gate source voltage.
- when the drain voltage is increase the positive drain potential opposes the gate voltage bias and reduces the surface potential in the channel
- the channel inversion layer charge decreases with increasing drain source voltage and ultimately it becomes zero when the drain source voltage is equals to (V_{GS}-$V_{GS(Th)}$)
- This point is called the channel pinch off voltage where the drain cureent becomes saturated