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Paper Computer Architecture

Department BSCS

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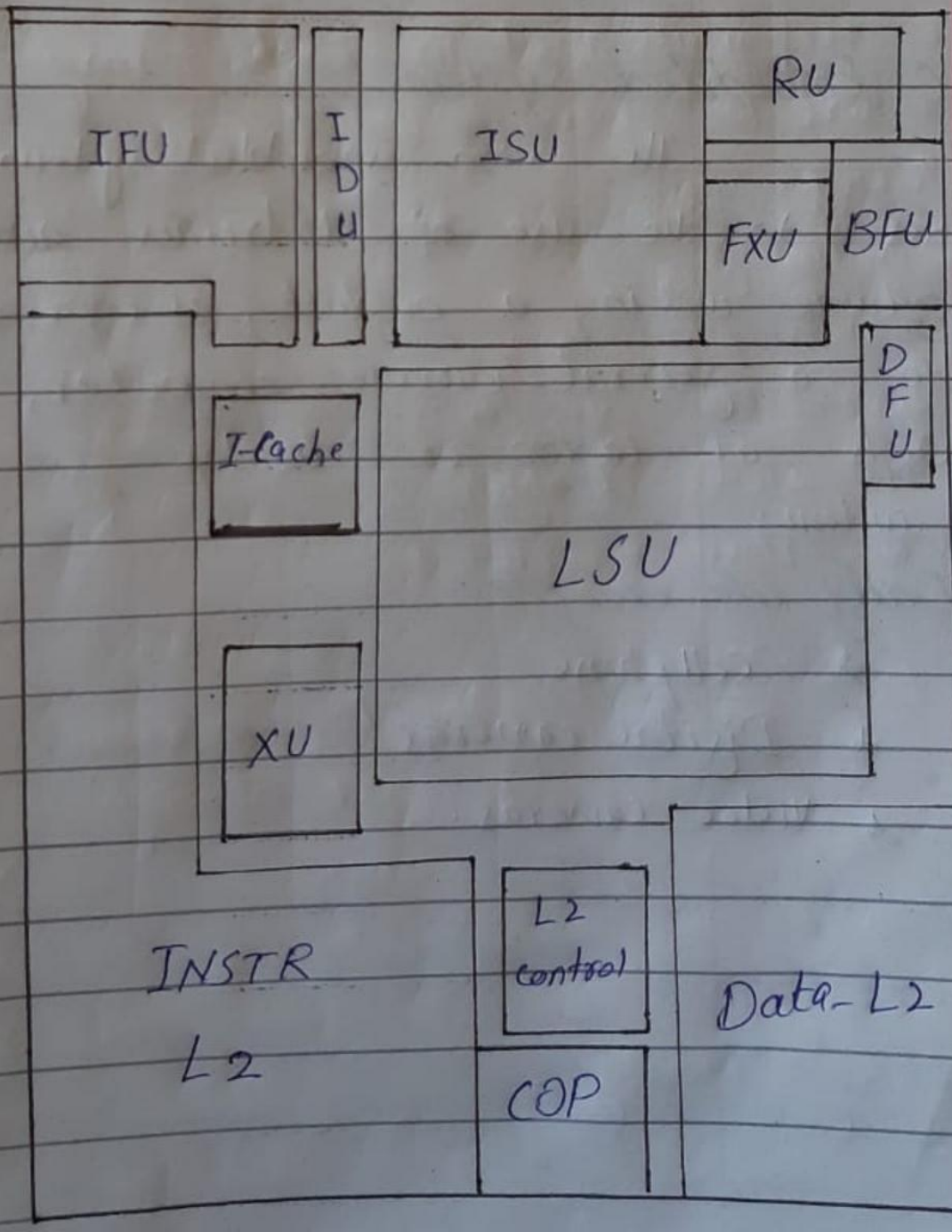
Q1 a)-



IDU :-

IDU is fed from the IFU buffers.

LSU :-

Responsible for handling all types of operand.

XU :-

Translate logical Address into physical Addresses in main memory.

FXU :-

Execute fixed point arithmatic operation.

BFU :-

Handles all binary and hexadecimal floating operations.

DFU :-

Handles both fixed & floating operations.

ISU :-

Determine the sequence in which instruction are executed.

IFU :-

Logic for fetching instructions.

RU:

keep a copy of the complete state of system.

COP:

Responsible for Data compression & encryption.

I-Cache:-

64-KB L_1 instruction coole

L_2 control:

Manages the trafic through L_2 cache.

Data L_2:

A1-MB L_2 Data cache for all memory trafic.

Instr-L_2

A1-MB L_2 instruction cache.

PART (B).

IAS Operation:-

The IAS operates by repetitively performing an instruction cycle. Each instruction cycle consist of the two subcycles.

(i) Fetch cycle

(ii) Execute cycle.

Fetch cycle:-

During fetch cycle the OP code of the next instruction is loaded into the IR & the address portion is loaded into the MAR.

Execute cycle:-

Control circuitry interpret the OP code & executes the instruction by sending out the appropriate control signals to cause data to be moved.

C- Embedded System:-

The term embedded system refers to the use of electronics and software with in a product, as opposed to a general-purpose computer, such as laptop or desktop system.

Daily life example:.

* Cellphone
* Digital cameras
* Video cameras.

D- Desktop Applications:-

* Image processing
* Three - dimensional rendering.
* Speech recognition.
* Video conferencing
* Multimedia authoring.
* Voice and video annotation of files.
* Simulation modelling.

E- Techniques:-

The techniques used in contemporary processors to increase speed are following.

* Pipelining
* Branch prediction.
* Super-scalar execution.
* Data flow analysis
* Speculative execution.

F- Increase in clock speed:-

problems created due to increase in clock speed and logic density of the processor are.

* Power
* Rc Delay
* Memory latency.

G- Amdahl's LAW:-

The speed up using a parallel processor with N processors that fully exploits the parallel portion of the program is as follows.

Speedup = Time to execute program on a single processor / Time to execute program on N parallel processor.

$= T(1-f) + Tf / T(1-f) + Tf/N =$

$1/(1-f) + f/N$

H- Multicore:-

* The use of multiple processors on the same chip provides the potential to increase performance without increasing the clock rate.
* Strategy is to use two simpler processors on the chip rather than one more complex processor.

MIC:-

* Leap in performance as well as the challenges in developing software to exploit such a larger number of cores.

GPU

* Core design to perform parallel operations on graphic data.
* Traditionally found on a plug-in graphic card, it is used to encode and render 2D & 3D graphics as well as process video.

I- QPI Protocol layer:-

In this layer, the packet is defined as the unit of transfer. One key function performed at this level is a cache coherency protocol, which deals with making sure that main memory values held in the multiple cache are consistent. A typical data packet payload is a block of data being sent to or from a cache.

J- Physical And logical Architecture of PCLE:-

A root complex device, also

refered to as a chipset or a host bridge, connects the processor and memory subsystem to the PCI express switch - fabric comprising one or more PCIe and PCIE switch devices.

2 Write a note on each of the following.

A- Main structural components :-

(i) CPU :-

Controls the operation of the computer and performs its data processing functions.

(ii) Main Memory :-

Stores data.

(iii) I/O :-

Moves data b/w the computer & its external environment.

(iv) System Interconnection :-

Some mechanism that provides for communication among CPU, main memory & I/O.

B- Key characteristics:-

(i) Similar or Identical Instruction set:-

In some cases, the lower end of the family has an instruction set that is subset of that of the top end of family.

(ii) Similar or Identical Operation sys:-

The same basic operating system is available for all family members.

(iii) Increasing speed:-

The rate of instruction execution increases in going from lower to higher family member.

(iv) Increasing No of I/O ports:-

Increases in going from lower to higher family member.

(v) Increasing memory size:-

Increases is going from lower to higher family member.

(vi) Increasing cost:-

The cost of the system is increases going from lower to higher family member.

C- Stored program Computer:-

A fundamental design approach first implemented in the IAS computer is know as stored-program concept. (John von Neumann) It consist of main memory which stores both data & instructions.

An arithmetic & logic unit capable of operating on binary data.

D- Moore's LAW:-

Number of transistors that could be put on a single chip was doubling every year.

Consequences of Moore's law:-

* Cost of computer and memory circuitry has fallen at a dramatic rate.
* The computer becomes smaller
* There is a reduction in power requirements.

E- INstruction Cycle state Diagram:-

* Instruction Address calculation
* Instruction fetch.
* Instruction operation decoding.
* Operand address calculation
* Operand fetch...
* Data operation.
* Operand store.

F- Classes:-

(i) Program:-

It is generated by some conditions that occurs as a result of instruction, execution.

(ii) Timer:-

It is generated by a timer with in the processor.

(iii) I/O:-

It is generated by an I/O controller.

(iv) Hardware failure:-

It is generated by a failure or memory parity errors.

Q-Bus Interconnection Scheme:-

The most common computer interconnection structures are based on the use of one or more system buses.

A system bus consist, typically, of from about fifty to hundred of separate lines. The lines can be classified into three functional groups:-

Data Address & control lines.

3 Differentiate each of the following:-

A) Computer Architecture	Computer Organization.
(i) Architecture describes what the computer does	Organization describe how it does it.
(ii) Computer Architecture deals with function behaviour of computer system.	computer organization deals with structural relationship.
(iii) Architecture indicates its hardware.	organization indicates its performance.

B) RISC | CISC

RISC	CISC
(i) The orignal microprocessor ISA	Redesigned ISA that emarge in the early 1980s.
(ii) Instructions can take several clock cycles.	Single cycle instructions.
(iii) More efficient use of RAM	Heavy use of RAM.
(iv) Large number Instructions.	Small number of fixed-length instruction.
(v) Compound Addressing modes.	Limited Addressing modes.

C- Microprocessor | Micro Controller.

Microprocessor	Micro Controller.
(i) Microprocessor is a heart of computer system.	Micro controller is a heart of embedded system.
(ii) Since memory and I/O has to be connected externally the circuit becomes	Since memory and I/O are present internally, the circuit is

large	small
(iii) cost of the entire system increases.	cost of entire system is low.
(iv) Mainly used in personal computers.	used in washing machine, MP3 players.

D-

	Cortex-A	Cortex-R	Cortex-M
Architecture profile	ARMv7-A ARMv8-A	ARMv7-R ARMv8-R	ARMv7-M ARMv8-M
Instruction set	32-bit/64bit	32-bit	32-bit
Interrupts	Software managed	Deterministic software managed	Hardware managed.
Operating system support.	Rich OS/RTOS	RTOS	RTOS.
Example processors	Cortex-A7 Cortex-A35	cortex-R8 cortex-R52	Cortex-M7 cortex-M33

E- Interrupt	without Interrupt.
In the interrupt cycle the processor check to see if anyone interrupts have occured, indicate by	if no interrupts are pending, the processor proceeds to the fetch cycle and fetches the

the presence of an interrupt signal.	next instruction of the current program.
F. Disable interrupt simply means that the processor can and will ignor that interrupt request signal. if an interrupt occurs during this time, it generally remains pending and will be checked by the processor after the processor has enabled interrupts.	Nested Interrupt. IS to allow an interrupt of higher priority to cause a lower-priority interrupt handler to be it-self ~~interrupte~~ interrupted. A user program beings at t=0 At t=10 a printer interrupts occurs, user information is placed on the system stack and execution ~~continues~~ continues at the printer interrupt service routine(ISR) while this routine is still executing at t=15, a communication interrupts occurs.

Q- Programming in Hardware & P. Software.

Hardware	Software.
* The "program" is in the form of hardware and is termed a hardware program.	The new method of programming which is a sequence of codes or instructions is called software programming.
* Suppose we construct a general-purpose configuration of arithmetic & logic functions. This set of hardware will perform various functions on data depending on control signals applied to the hardware. Inthis original use of customized hardware the system accepts data & produces results.	* In this method programming is much easier, instead of rewiring the hardware for each new program, all we need to do is provide a new sequence of codes. Each code is, in effect, an instruction and part of hardware ~~interrupts~~ interprets each instruction and generates control signals.

4 A- Solution:-

① LH instruction = 010FA
OPcode = 0FA
RH Instruction = 210FB
OP code = 21
address = 0FB

This is a hexadecimal form you have to convert the numbers to binary form.

(use IAS instruction set)

LH instruction.

01 = 00000001 = LOAD M(X)

M(X) refers to memory address location 0FA

The first 8 bits of 08A should read - LOAD M(0FA)

RH Instruction.

21 = 00100001 = STOR M(X)

M(X) refers to the memory address location 0FB.

The second 8bit of 08A should - read STOR M(0FB)

Finally the assembly language code for 08A 010FA210FB is

LOAD M(0FA)
STOR M(0FB).

② Contents are divided up into two 5 bit instructions, LH & RH.

LH instruction = 010FA

OP code = 01

address = 0FA

RH instruction = 0F08D

OP code = 0F

address = 08D.

This hexadecimal form convert into binary form.

LH instruction:-

01 = 00000001 = LOAD M(x)

M(x) refers to the memory address location 0FA.

The first 5 bit of 08B should read- LOAD M(0FA).

RH instruction:-

0F = 00001111 = Jump + M(x, 0:19)

refers to the memory address 08D.

The second 5 bits of 08B should- read - jump + M(08D, 0:19)

Finally the assembly language code for 08B 010FA0F08D is

LOAD M(0FA)

Jump + M(08D, 0:19).

3-

LH instruction = 020FA

OP code = 02

address = 0FA

RH instruction = 210FB

Op code = 21

address = 0FB

This is in hexadecimal form we convert to binary form.

LH instruction:

02 = 00000010 = LOAD- M(x).

M(x) refers to memory address location 0FA.

This first 5 bits of 08C should read - LOAD - M(0FA).

RH instruction:-

21 = 00100001 = STOR M(x)

M(x) refers to memory address location 0FB.

The second 5 bits of 08C should read - STOR M(0FB).

Finally the assembly language code for 08C 020FA210FB is

LOAD - M(0FA)

STOR M(0FB).

b- what this program does:-

In 08A address the M(0FA) transfer to the accumulator and transfer contents of accumulator to the memory location 0FB.

In 08B address the M(0FA) transfer to the accumulator and take next instruction from left half of M(08D).

In 08C address the M(0FA) transfer accumulator and transfer contents to memory location (0EB).

PART-B

ANSWER:-

(a) Opcode = 00000001

Operand = 000000000010

(b) In, the beginning, the CPU have to fetch the instruction from the memory. Then, the instruction will include the address of the data which is required to load. Through the execution time, the memory will be accessed in that time to load the data contents which is located at that address for a total of two trips to memory.

PART C.

Effective CPI's :-

$$CPI = (1 \times 46000) + (2 \times 33000) + (2 \times 16000) + (2 \times 8000)/100$$

$$CPI = 162000/100$$

$$CPI = 1620$$

MIPS :-

$$\text{MIPS rate} = 60\,MHz / 1620 \times 10^6$$

$$\text{MIPS rate} = 60 \times 10^6 H_2 / 1620 \times 10^6$$

$$= 60 H_2 / 1620$$

MIPS rate = 0.037

Execution Time :-

$$T = I_c / (MIPS * 10^6)$$

$$T = 104000 / (0.037 \times 10^6)$$

$$T = 104000 / 37 \times 10^3$$

$$T = 2811 \times 10^{-3}$$

T = 2.811sec.

PART-D

D Solution:-

(a)

Instruction Type	CPI	Instruction Mix
Arithmetic & Logic	1	60%
Load/Store with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	12	10%

The Average CPI = (1 × 0.6) + (2 × 0.18) + (4 × 0.12) + (12 × 0.1) = 2.64

Therefor CPI has been increased since the

time for memory access is also increased.

(b) MIPS = 400 / 2.64 = 152

There is corresponding drop in the MIPS rate.

(c) $T = Ic / (MIPS \times 10_6)$

For the one processor,

$T_1 = (2 \times 10_6) / (178 \times 10_6) = 11ms$

For the 8 processors each processor execute 1/8 of the 2 million instructions plus the 25,000.

$T_8 = 2 \times 10_6 \div 8 + 0.025 \times 10_6 / 152 \times 10_6$

$T_8 = 1.8ms$

Speedup = 11/1.8

speedup = 6.11.

(d) By depending on the information given, it is not obvious how to quantify this effect in Amdahl's equation. Therefore if it is supposed that the fraction of code, which is parallelizable, is $f = 1$, then Amdahl's decreases to speed-up = N = 8, Therefore the actual speed up is only 75% of the theoratical speed up.

E

PART : E

(i) (a) The PC contain 300, the address of the first instruction. This value is loaded into the MAR. (b) The value in location 300, is loaded into the MBR and the PC is incremented. The two steps can be done in parallel &. (c) The value in the MBR is loaded into the IR.

(ii) (a) The address portion of the IR (940) is loaded into the MAR. (b) The value in location 940 is loaded into the MBR. & (c) The value in the MBR is looked into the AC.

(iii) (a) The value in the PC (302) is loaded into the MAR. (b) The value in location 302 is loaded into the MBR and PC is incremented (c) The value in MBR is loaded into the IR.

(iv) (a) The address portion of IR is loaded into the MAR. &. (b) The value in location 941 is

loaded into MBR ©. The old value of the ac & the value of location MBR are added & the result is stored in the AC.

(v) (a) The value in the PC (302) is loaded into the MAR. (b).

(b) The value in the location 302 is loaded into the MBR & the PC is incremented (c).

(c) The value in the MBR is loaded into the IR.

(vi) (a) The address portion of the IR. 941 is loaded into MAR. (b). The value in the MBR is stored in the location 941.

PART F.

Answer:-

(a) $2^{24} = 16$ MBytes.

(b) (i) if the local address is 32bit the whole address can be transfer at once and decoded in memory, However the data bus in only 16 bits, it will requires 2 cycle to fetch a

32 bit instruction or operand.

(ii) The 16 bits of the address placed on the address bus can't access whole memory. Thus more complex memory interface control is needed to latch the first of the address & then the second part.

(c) The program counter must be atleast 24 bits, Typically 32-bit microprocessor will have a 32-bit external address bus and a 32-bit program counter, unless on chip segment registers are used that may work with a smaller program counter. If the instruction register is to contain the whole instruction it will have to be 32-bits long; if it will contain only the OP code (called the OP code register) then it will have to be 8-bits long.

PART G.

A bus cycle takes 0.25μs, so a memory cycle takes 1μs. If both operands are even aligned it takes 2 μs to fetch the two operands. if one is odd aligned the time required is 3μs. If both are odd aligned, the time required is 4μs.