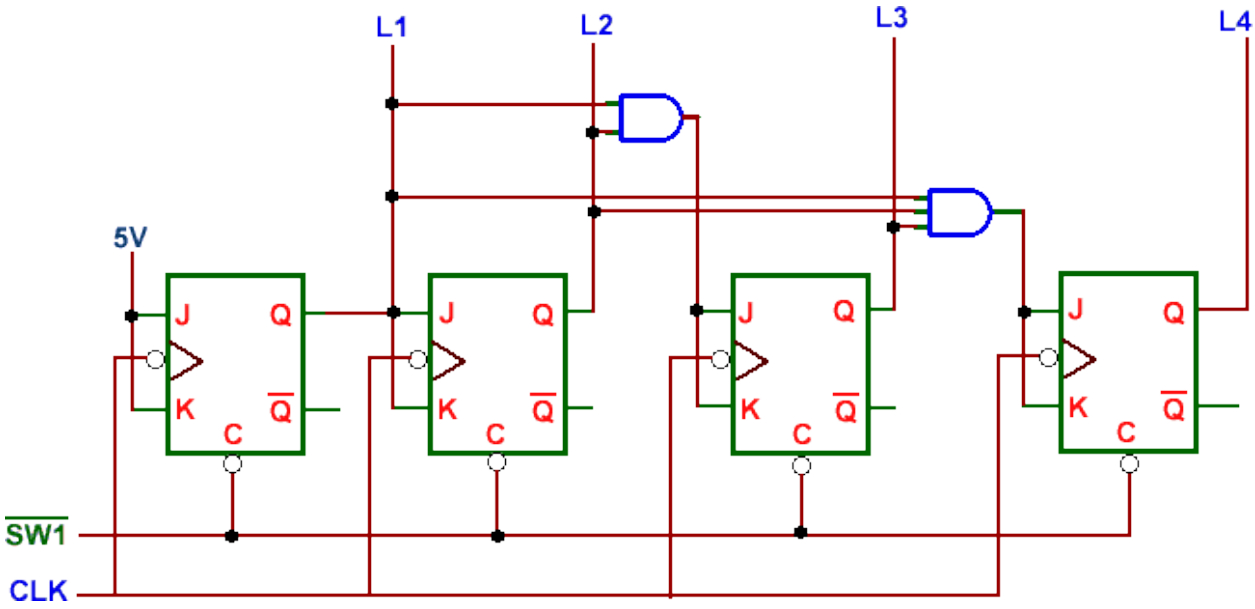
Name:
Muhammad Bilal Elahi
ID:
15434
Department:
Computer science
Submitted to:
Sir Muhammad Amin

Synchronous Counters

Synchronous counters eliminate the cumulative flip-flop delay seen in ripple counter. Each flip-flop is clocked by the same clock signal. Each gate selectively controls when each more significant bit flip-flop is to change state (toggle) on the next clock transition. Such control (enable) can be realized by setting, for example, the J and K inputs of a J-K flip-flop. Because of this control, the addition of a common clock will synchronize data transfer and all flip-flops will change state simultaneously. The important feature of a synchronous counter is that the transitions of the individual flip-flops are synchronized to a master clock signal.

J-K flip-flops are normally used in the synchronous counters due to the enabling (controlling) feature of the J and K inputs. There are two basic schemes for generating the J and K inputs. One of them is illustrated in the four-bit binary counter shown in Fig. 2. Notice that the information to the J-K inputs is formed in a parallel fashion. The counter is accordingly termed as synchronous parallel counter. In the parallel scheme the number of inputs to each AND gate increases linearly with the number of stages. For this added expense one gets the fastest possible synchronous counting circuit.



If the J-K input information is formed from the output of the AND gate in the previous stage, one has a synchronous serial counter. Although the serial scheme is slower than the parallel scheme, the number of inputs to the AND gate per stage is constant in the serial case (two inputs per stage).

2. Experiments

Connect the count-up ripple counter shown in Fig. 1 using two 74LS76 chips. Set data switch SW1 from logic 0 to logic 1 (clear all flip-flops). Now connect CLK to a pulse generator in your pencil box (J-K flip-flops in 74LS76 are negative edge triggered) and start counting by pushing the pulser button. Continue the process and record the output of each transition in a truth table. Does it count correctly?

We can convert the count-up ripple counter to a count-down ripple counter by connecting the clock of the flip-flops to Q instead of Q (the LEDs are still connected to Q). Make the modification and try out the circuit.

Connect the 4-bit synchronous parallel counter as shown in Fig. 2. Repeat the same procedures in the ripple counter experiment. From the transition table of the counter and the excitation table of the J-K flip flop, verify that the J-K inputs to the flip flops are correct.

4. Equipment and parts required

- Protoboard
- Two JK Flip-Flops (74LS76)
- One 3-input AND (7411)

Conclusion:

Synchronous Counter is verified.