(1)

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(2)

(a) EEPROM and flash memory :-

flash memory is one kind of non-volatile random-access memory. it is slower than RAM but faster than hard drives ... The main different between EEPROM and flash memory is that most EEPROM devices can erase any byte of memory at any time. Flash memory can only erase on entire chunk or "Sector" of memory at a time flash memory is used primarily for storage, while RAM (random acces memory) perform calculations on the data retrived from Storage. By their nature flash memory and RAM are faster than storage alternatives such as hard disk and tape in terms of flash memory.

Q2 (b)

Ans: In this content hard failures are errors that occur through process defects and/or circuit bugs - hard failures are repeatable with the Correct Sequence of action within the microcontroller Soft errors

(2) (3)

Soft errors occur through no failure of the circuit or defect but due to an external source that causes the data to change.

(12) (C)

Disk read / write heads are the small parts of a Disk drive which move above the disk platter and transform the platter's magnetic field into electrical current (read the disk) or, vice versa are transform electrical current into magnetic field (write the disk)

(12 E :-

Explanation:-

Blue-ray and HD DVD both uses a blue laser which has a shorter wavelength than red ones. In contrast; HD. DVDs can hold 25 GB on one layer. Even more can be packed into Blue-ray / HD DVD discs if they use more than one or one side of the disc.

(3) (4)

"D"

Parallel And Independant Access RAID Schemes.

→ PARALLEL Access.

→ RAID levels 2 and 3 makes use of a parallel access technique.

→ In a parallel access array RAID returns all numerber disk participate in the execution I/O request.

→ Typically the Spindles of the individuals drive are Synchronized So Such disk head is in the Same position on Such disk at any given time

Independant Access:-

→ RAID level 4 utilize independant Access technique.

→ Each number disk operate ~~monitor~~ disk independant enlike.

RAID 2 and 3.

→ In independant access Such are member disk operates independently So that Separate I/O request Can be Satisfied in parallel.

(1) No 1

(9)

Word:-

The natural unit of organization of memory - th size of a word is typically equal to the number of bits used to represent an integer and to the instruction length Importunately, there are many exceptions for example the CRAY (8s has a 64-bit word length but uses a 46-bit integer representation the intel x86 architectures has a wide variety of instruction lengths expressed as multiple of bytes and a word size of 32 bits.

Addressable unit:

In Same ten Systems the addressable unit is the wood. Hower many Systems allow addressing at the byte level in any case the relationship between the lengths in bits. A of an addren enel is

$$2^A = N$$

unit of transfer:-

for main memory this in the number of bits read out of or written into memory at a time the unit of transfer need not equal a word or an addressable unit - for external memory data are often transferred in much larger units than a word and these are referred to as block.

Ans (b)

least Recently used (LRU):

~~LFU contd~~

least Recently used (LRU) is easily implemented by two-way Set ere associative mapping Each line include a USF bit. when a line is referenced. its use USE bit is set to 1 and USE bit of the other line is that set. is set to 0.

When a block is to be read into the set. the line whose USE bit is 0 is used Because we are assuming that more recently used ~~more~~ memory location are more likely

likely to be referenced (LRU) should give the best hit ratio.

least frequently used (LFU):

LFU could be are implemented by associating a counter with each line. A technique not based an usage (i.e not LRU. LFU. FIFO or same variant) is to pick a line at random from among the candidate lines. Simulation studies have shown that random replacement provides only slight inferior performance to an algorithm based on usage.

Ans(d) all

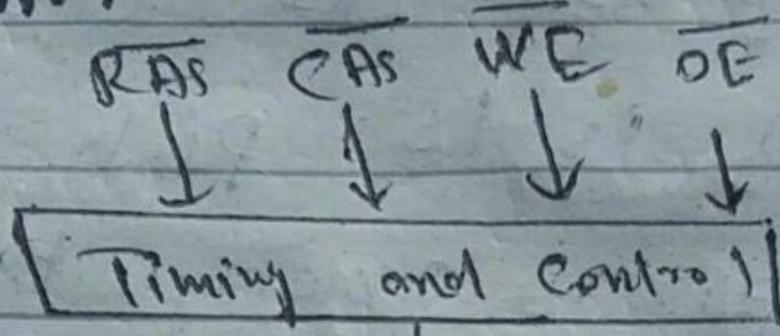
16 - Mibit DRAM:-

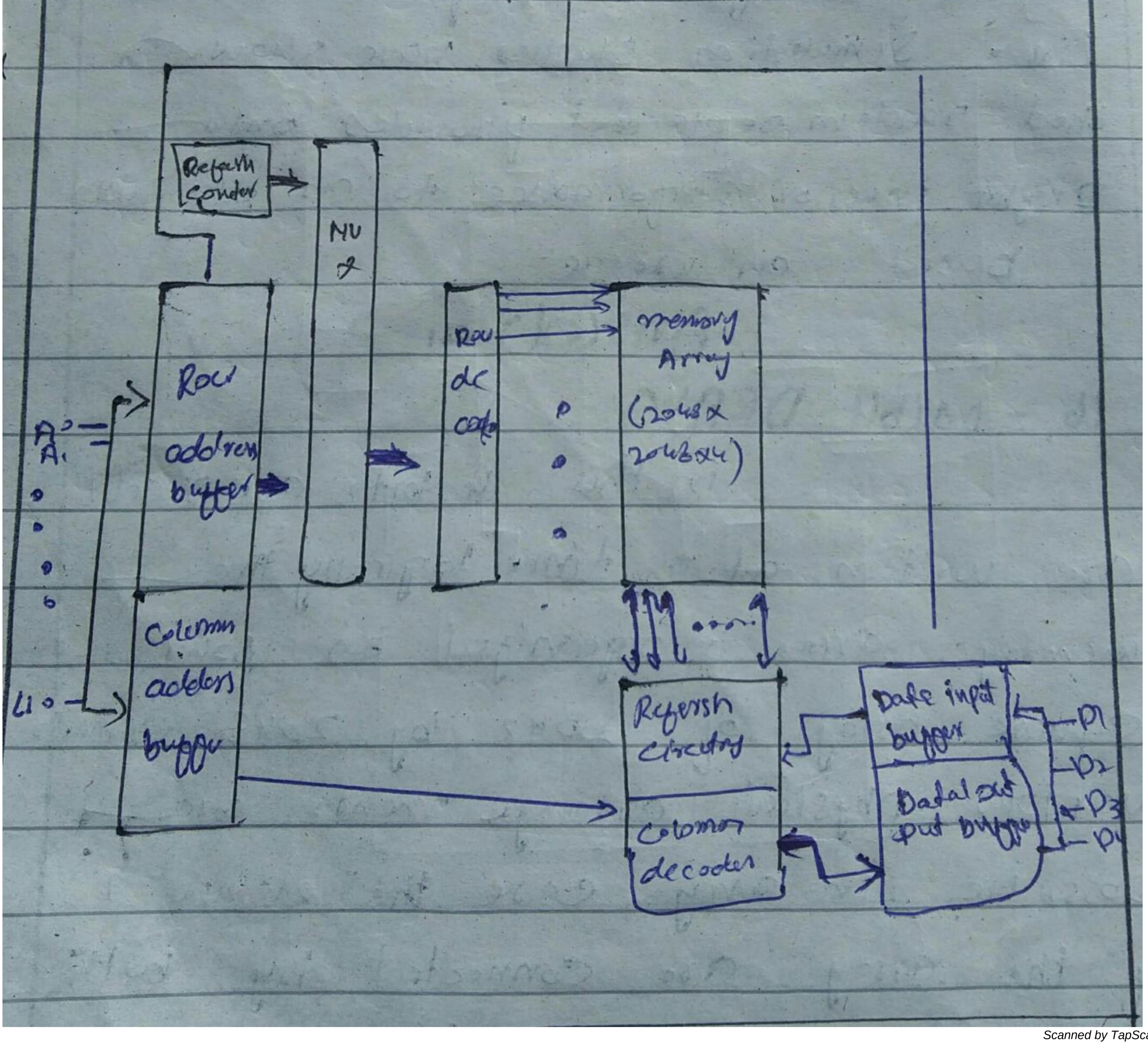
In this 4 bits are read/ are written at a time logically the memory array is organized as four square arrays of 2048 by 2048 elements various physical arrangements are possiable in any case the elements of the array are connected by bolth horizental line connects to the select terminal of each cell in its row each vertical lines connects to the Data

Sense terminal of each cell in its column

Because only 4bits are read / written to this DRAM there must be multiple DRAMs connected to the memory controller to read / write a word of data to the bus.

Diagram:-





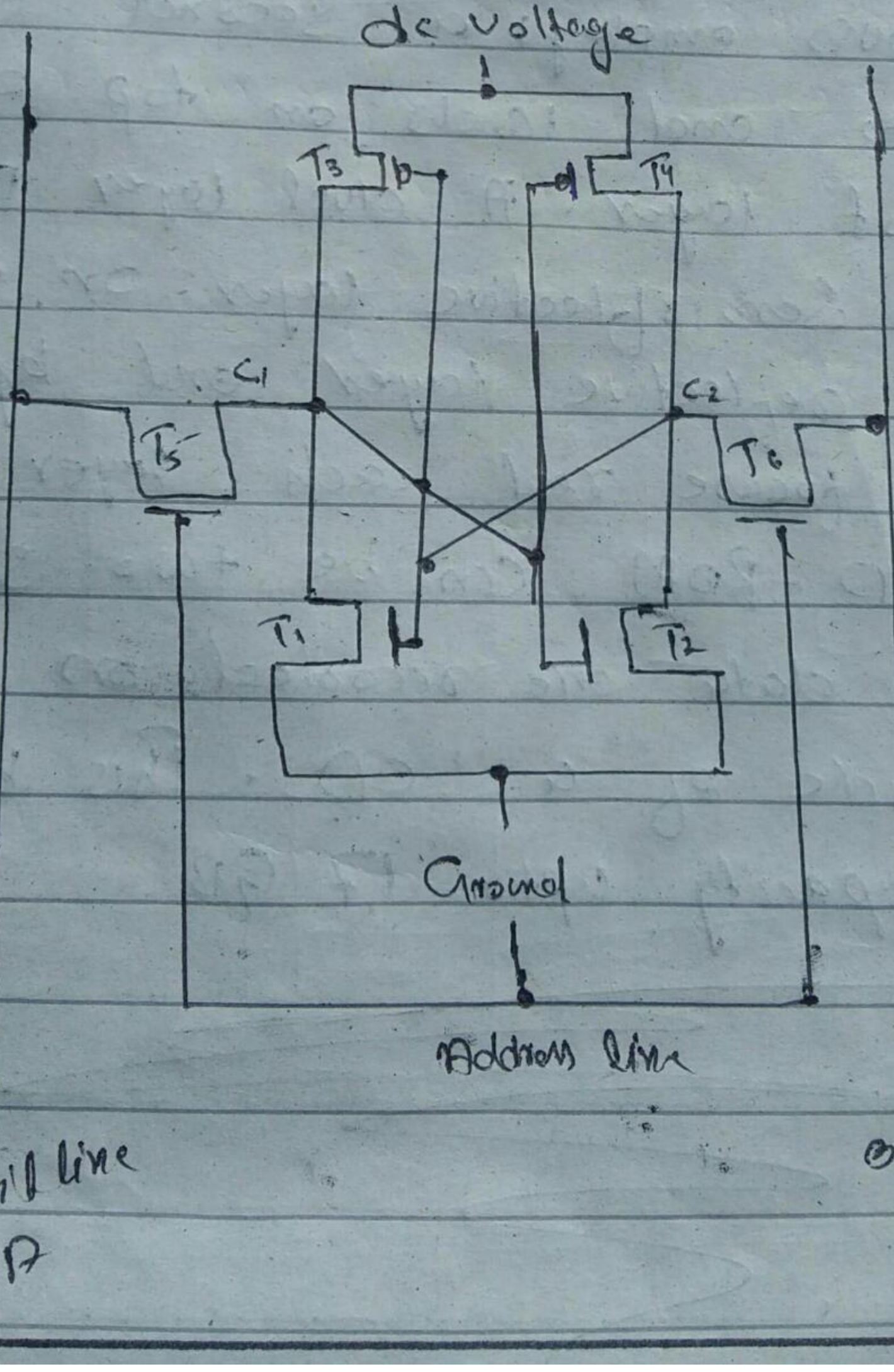
An "C" cell

Read operation:-

In SRAM for only operation to be performed the word line should be high To perform read operation initially

write operation :-

Consider the memory bits consists of Q = 0 and Q' = 1



(9)

Ans (E)

The DVD greater capacity is due to there diferents form CDs.

(1) Bits are packed more closely - on a DVD the spacing between loops of a spacing between on a CD is 1.6 μm and the minimum distance between pits along the spiral is 0.834 μm

(2) The DVD employs a second layer of pits and lands on top of the first layer. A dual layer DVD has a semireflective layer on top of the reflective layer and by adjusting focuse real each layer separatly.

(3) The DVD-ROM can be two sideal however data are recodeed on only one side of a CD. This brings total capacity upto 17 GB

(13) (9)

Memory Access Methods:-

* Sequential Access:-

Memory is organized into units of data called records Access must be made in a specific linear Sequence Stored addressing information is used to Separated Second and assist in the retrival process A Shared read-write mechanisem is used and this must be moved from it Current location to desired location passing and rejecting each intermediat record

Tape units are Sequential access.

* Direct Access:-

As the Sequential access direct access invales a shared used write mechanism However individual blocks or records have a unique are adolsess based on physical location Access time is variable. Dist units are direct access.

* Random Access:-

The time to Access a

given location is independent of the Sequence of prior accesses and is are constant. Thus any location can be Selected at random and directly addressed and accessed. Main memory and Same cache Systems are random access.

* Associative Access:-

This is a random access type of memory that enables one to make a comparison of desired bit location within a word for a Specified match and to do this for all words Simultaneously thus a word is retrived based on a portion of its contents rather than its address Cache memory may employ associative access.

" b "

Principle of locality:-

The principle of locality states that data in the vicinity of a referenced word are likely be referenced

(a) Temporal locality:

It refer to the re use of Specific data and/or resources within a relatively small time duration.

(b) Spatial locality:-

it as also known as data locality. It refers to the use of data elements within relatively close storage location.

Q3(C)

Possiable approaches to cache Coherency

possable Approach to cache conerency includes the following

- Bus watching with write through:- Each cashe Controller monitors the address lines to detect writes operation to memory by other bus master another master written to a location shared memory that also resides in the cache memory.

- Hardware Transparency:-
  Additional hardware use to ensure that all update to main memory via cache are reflected in all caches.
- Non cacheable Memory:-
  only a portion main memory is shared by more then one processor and the non cacheable memory can be identified using chip-select logic or high address bits.

Q3(e)

Ans:-

Read:

Information is retrieved from CD or CD-ROM by a low-powered laser housed in an optical disk player or drive unit. The laser shines through clear polycarbonate while a motor spins disk past it. The intensity of the reflected of the light

laser changes as it encounters
effect of Specially the laser
beem fall on a pit which has
a Some what rough surface
the light Scatters and a low
entensity. ~~reco~~ recod

Write :-

Recall that on a megnetick
disk Information is record concen
tric tracks with simplest constant
angular velocity ((AV) System
the numer of bits per track
is Constent. An increase indens-
city achived with multiple zoned
recording.

Although this techinepe increase
Capacity it is not still not
optiamel.

Q3 (D)

Partical issues pecular to SSD

There are two paritical issues pecular to SSDs that are not faced by HDDs.

(1) first SSD performence has a tendency to slow down for this device is used to known that files are stored on disk as a set of moves disk as set of pages typially 4KB in length those pause are not.

necessely onel indeed not are typically stored as a cortegus set of pases on the disk.

(2) A second purticel issues with flash memory drives is that a flash memory become ensable after a that become.

(Q) No 4

(a)

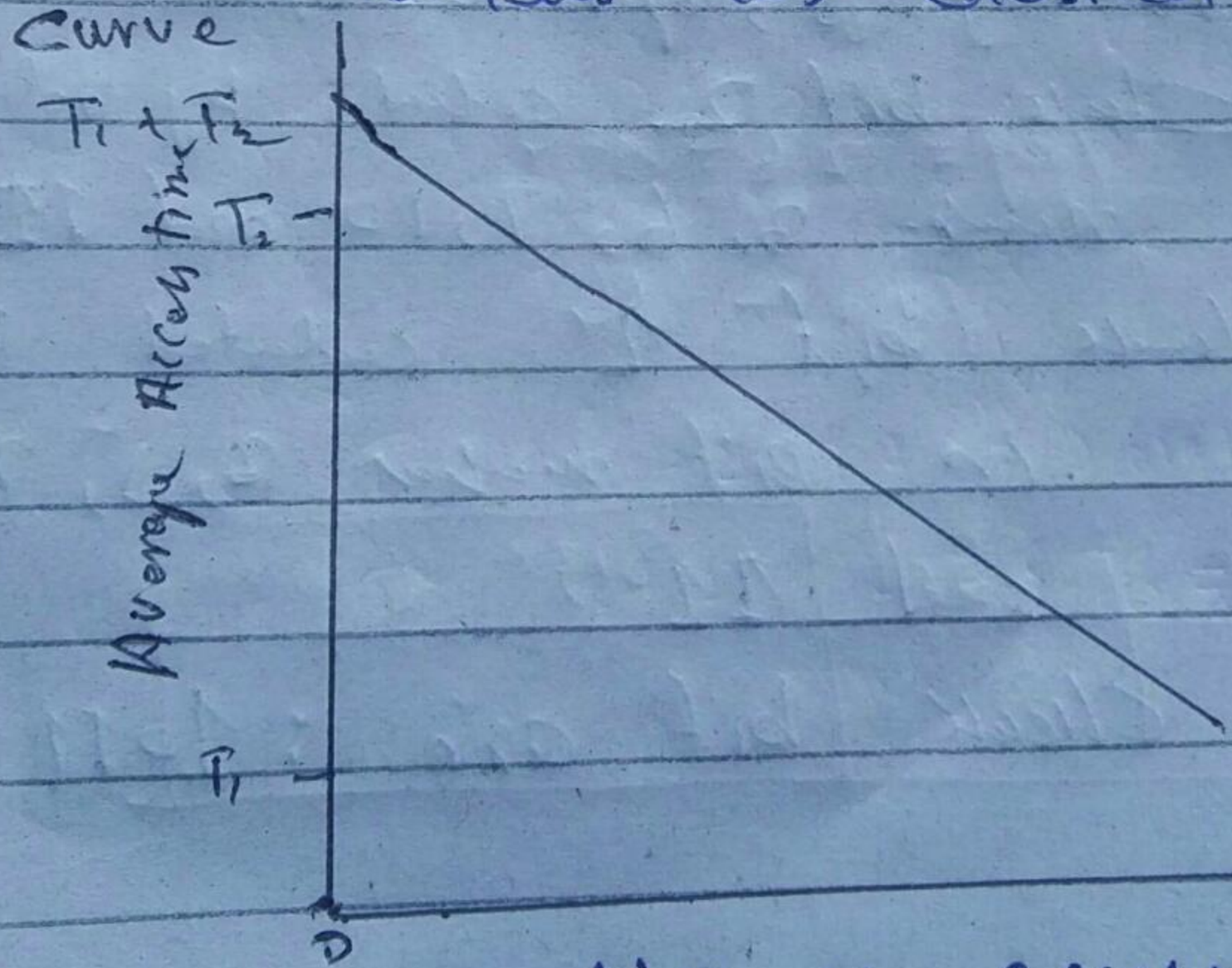
in example suppose 95% of the memory accesses the average time to access a word can be exposed as

$(0.95)(0.01\mu s) + (0.05)(0.01\mu s) + 0.1\mu s)$

$= 0.00095 + 0.00055$

$= 0.015\mu s$

The average access time is much closer to $0.01\mu s$ than $0.1\mu s$ as desired



Function of accesses involving any level 1 (hit ratio)

Q 4 (c)

M = 8

$2^{-1} >= 1 + n$

$2^4 - 1 >= 4 + 8$

$15 >= 12$

1	2	3	4	5	6	7	8	9	10	11	12
1	0	1	1	1	0	0	1	0	0	1	0

The check bits are in a bit numbers 1, 2, 4, 8 & check bit 8 calculated By value in bit number 9, 10, 11, and 12

Che bit 4 calcet by value in number = 5, 6, 7 and 12

Check bit 2 calcul. by value bit num. 3, 6, 7, 10 and 11

Check bit 1 calculated by value in Bit number 3, 5, 7, 9, 10 and 11.

The check bit are : 1011

Q 4 (d)

Sol:-

7200 revaluation in 60 sec

1 reva. in 60/7200

1 revolution in 6ms

1 revolution covering one entire tract 500 sector

500 Sector = 6ms

1 sector = 8 microsecond

Now there are 2 different thing

① 2500 Sectors so time = 2500 × 8ms

= 20ms

② 1.28mB = 1342177 28 Bytes OR 2601.44 Sector 2622 sector = 20.976ms

Total Time Case

Case ① 4+2+20 = 26ms

Case ② 4+2+20.976 = 26.976ms

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(3) No 4 (B)

Total block in the cache

= 8 Kbyte / 16 bytes = $2^3 \times 2^{10} / 2^4$

$\Rightarrow 2^9 = 512$

Number of Set = number of block in Cache

Number of Set = 512/2

Number of set in cache = 256

Num of Set = 8

Size block = 16 = 2^4

Size of memory = $2^6 \times 2^{20} = 2^{26}$

Tag = Siz of mem - Set-size + block

Tag = 26 - 8 - 4

Tag = 14

Tag	Set	Size of block
14	8	4