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Sessional Assignment No : 5th

Subject : Computer Architecture

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Assignment No : 05

Q1:-

Ans:(a) There are various types of semiconductor memories. The most common is referred to as RAM (random access memory). Most types have the property of RANDOM ACCESS MEMORY which means that it takes the same amount of time to access any memory location.

Here is a table of semiconductor memory types.

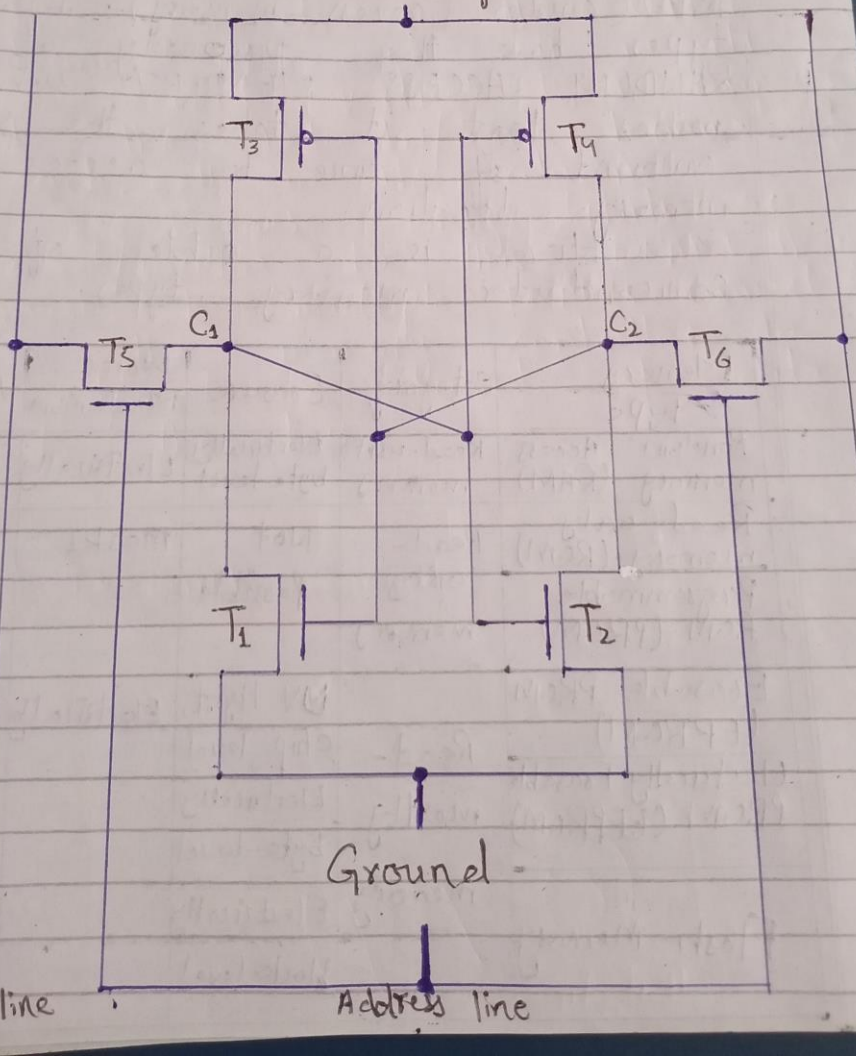
Memory Type	Category	Erasure	Write Mechanism	Volatility
Random Access memory (RAM)	Read-write memory	Electrically, byte-level	Electrically	Volatile
Read-only memory (ROM)	Read-only memory	Not possible	Masks	Non-volatile
Programmable ROM (PROM)				
Erasable PROM (EPROM)		UV light, chip level	Electrically	
Electrically Erasable PROM (EEPROM)	Read-mostly memory	Electrically, byte-level		
Flash Memory		Electrically, block-level		

Ans: (b) **Read Operation:-**

In SRAM, for any operation to be performed, the word line should be high. To perform read operation, initially.....

Write Operation:-

Consider the memory bits consists of $Q = 0$ and $Q' = 1$.

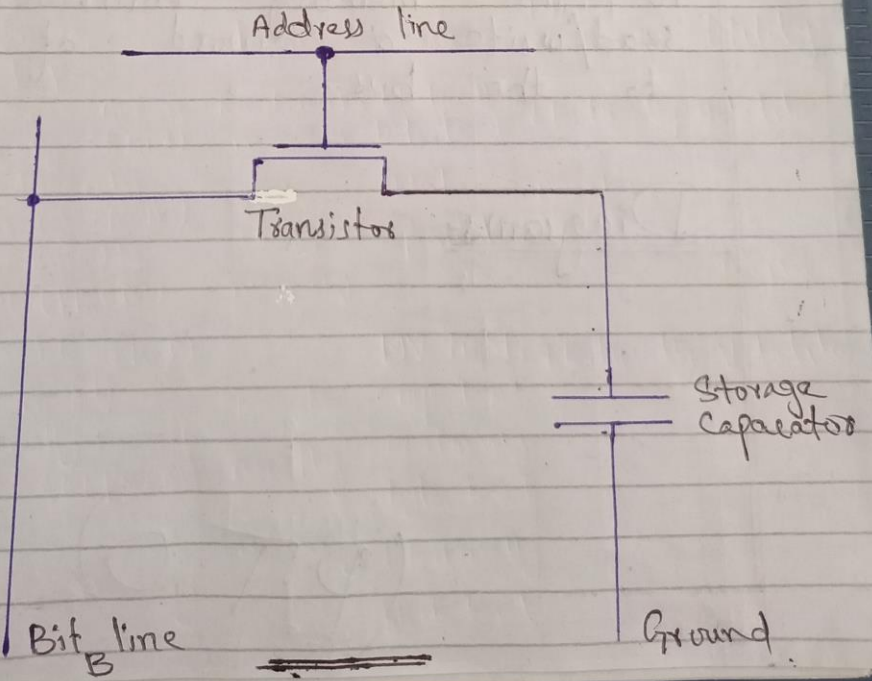


Ans: (c) **Read Operation:-**

The address line is activated when the bit value from this cell is to be read or written. The transistor acts as a switch that is closed if a voltage is applied to the address line and open if no voltage is present on the address line.

Write Operation:-

A voltage signal is applied to the bit line, a high voltage represents 1, and a low voltage represents 0. A signal is then applied to the address line allowing a charge to be transferred to the capacitor.



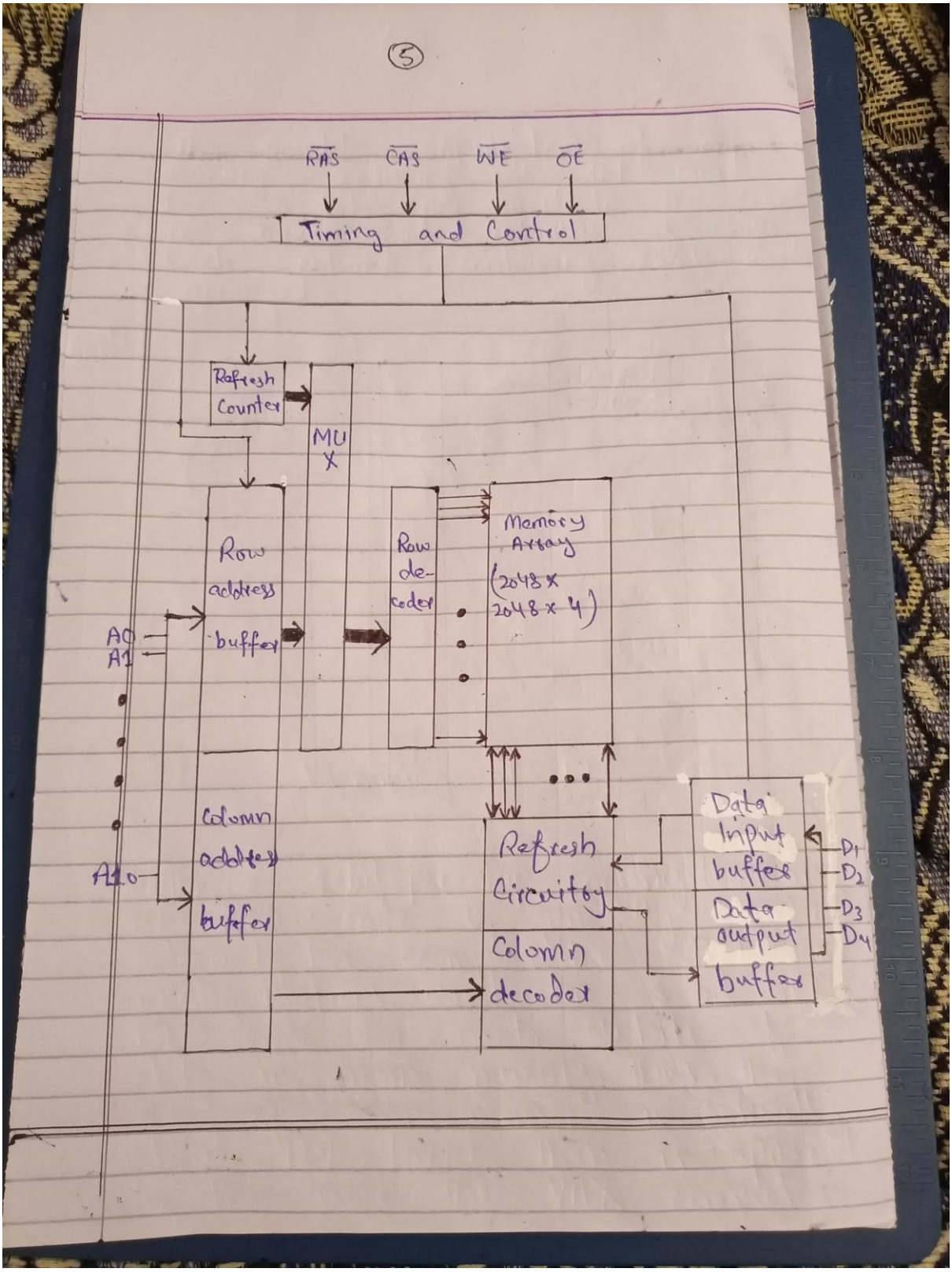
Ans: (d) 16-Mbit DRAM:-

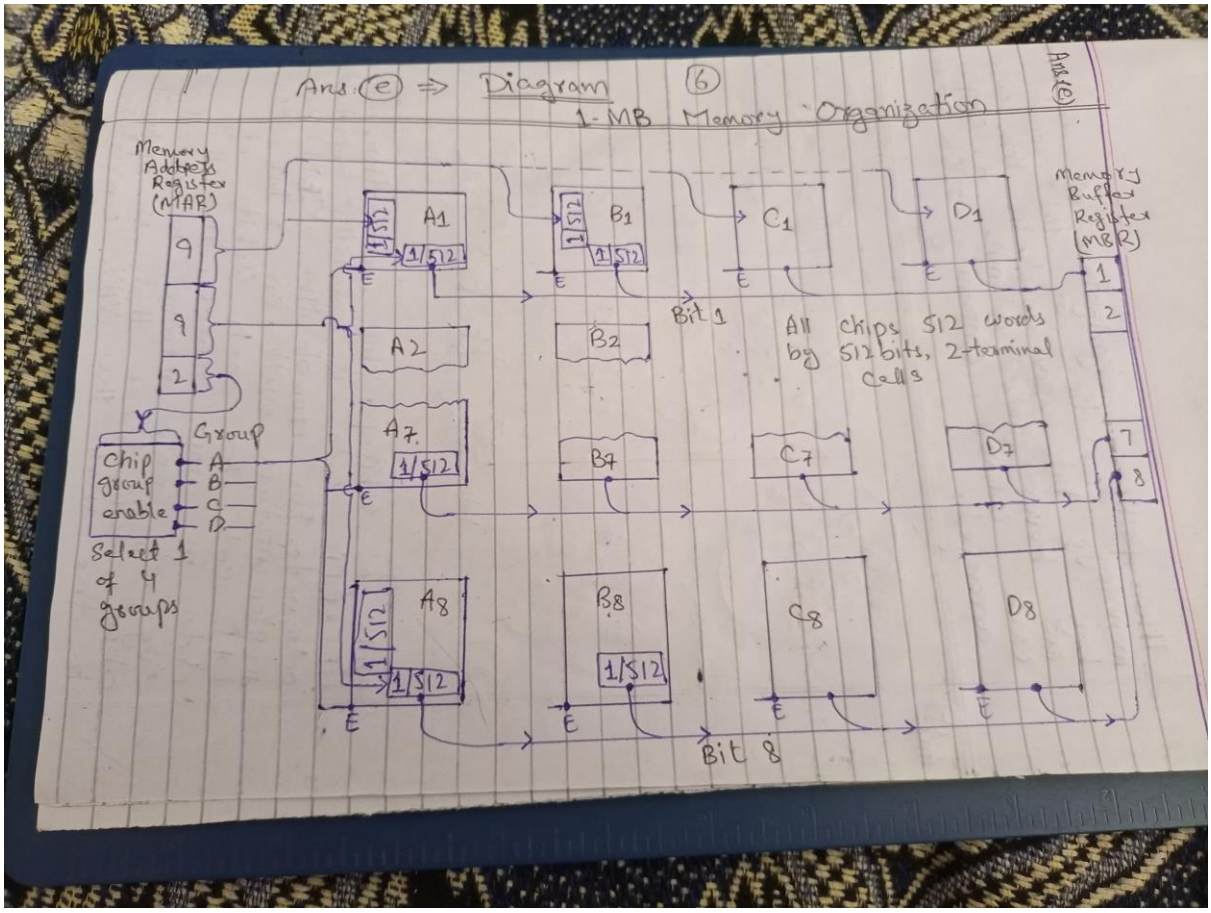
In this case, 4 bits are reads or written at a time. Logically, the memory array is organized as four square arrays of 2048 by 2048 elements. Various physical arrangements are possible. In any case, the elements of the array are connected by both horizontal and vertical lines. Each horizontal line connects to the select terminal of each cell in its row; each vertical lines connects to the Data-In/Sense terminal of each cell in its column.

Because only 4bits are read/written to this DRAM, there must be multiple DRAMs connected to the memory controller to read/write a word of data to the bus.

Diagram:-

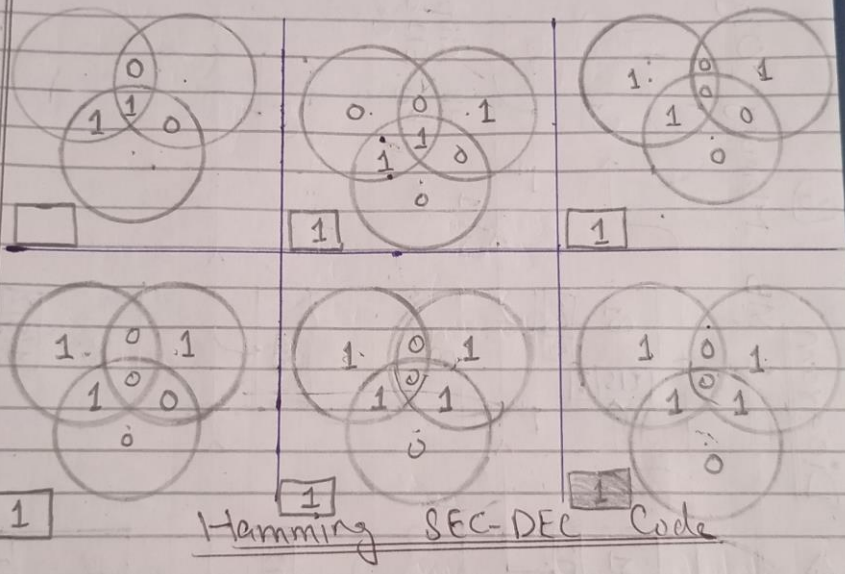
(P.T.O)


RAS
CAS
WE
OE
Timing and Control
Refresh Counter
MUX
Row address buffer
Row de-coder
Memory Array (2048 x 2048 x 4)
A0
A1
A10
Column address buffer
Refresh Circuitry
Column decoder
Data input buffer
Data output buffer
D1
D2
D3
D4


Ans: (e) ⇒ Diagram (6)
1-MB Memory Organization
Ans (e)
Memory Address Register (MAR)
9
9
2
Y
Group
Chip group enable
A
B
C
D
Select 1 of 4 groups
A1
B1
C1
D1
A2
B2
A7
B7
C7
D7
A8
B8
C8
D8
1/512
E
Bit 1
Bit 8
All chips 512 words by 512 bits, 2-terminal cells
Memory Buffer Register (MBR)
1
2
7
8

The possible organization of a memory consisting of 1M word by 8 bits per word. In this case we have four columns of chips, each column containing 256k words arranged.

Ans: (f)



Hamming SEC-DEC Code

With a 1-bit-per-chip organization, an SEC-DED code is generally considered adequate. For example, the IBM 30xx implementations used an 8-bit SEC-DED code for each 64 bits of data in main memory. Thus, the size of main memory is actually about 12% larger than is apparent to the user. The VAX computers

used a 7-bit SEC-DED for each 32 bits of memory. for a 22% overhead. Contemporary DRAM system may have anywhere from 7% to 20% overhead.

Ans. (9) Syndrom for the Hamming code interpreted as follows;

(*) If the syndrome contains all 0s, no error has been detected.

(*) If the syndrome contains one and only one bit set to 1, then an error has occured in one of the 4 check bits. No correction is needed.

(*) If the syndrome contain more than one bit set to 1, then the numerical value of the syndrome indicates the position of the data bit in error. This data bit is inverted for correction.

Q2.

Ans. (a) DRAM:-

A dynamic RAM (DRAM) is made with cells that store data as charge on capacitors. The presence or absence of charge in a capacitor is interpreted as a binary 0 or 1. Because capacitors have a natural tendency to discharge, dynamic RAMs

require periodic charge refreshing to maintain data storage. The term dynamic refers to this tendency of the stored charge to leak away, even with power continually applied.

SRAM:-

A Static RAM (SRAM) is a digital device that uses the same logic elements used in the processor. In a SRAM, binary values are stored using traditional flip-flop logic-gate configurations. A static RAM will hold its data as long as power is supplied to it.

Ans (b) EEPROM:-

Electrically erasable programmable read-only memory (EEPROM) is a read-mostly memory that can be written into at any time without erasing prior contents only the byte or bytes addressed are updated. The write operation takes considerably longer than the read operation. EEPROM is more expensive than EPROM and also is less dense, supporting fewer bits per chip.

Flash memory:-

Flash memory is intermediate between EPROM and EEPROM in both cost and functionality. Like EEPROM, flash memory uses an electrical erasing technology. An entire flash memory can be erased in one or a few seconds, which is much faster than EPROM. Flash memory does not provide byte-level erasure.

Ans:(c) Hard Failure:-

A hard failure is a parmanent physical defect so that the memory cell or cells affected cannot reliably store data but become stuck at 0 or 1 or switch erratically between 0 and 1. Hard errors can be caused by harsh environmental abuse, manufacturing defects, and wear.

Soft errors:-

A soft error is a random, nondestructive event that alters the contents of one or more memory cells without damaging the memory. Soft errors can be caused by power supply problems or alpha particles. Both hard and soft errors are clearly undesirable.