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Assign 02 chap

Sems 4th

Q1 part A

Different desktop applications that require the Great power of Contemporary microprocessor based System are:
Image processing.
Three dimensional rendering.
Speech recognition
Video conferencing
Multimedia authoring
Voice and video annotation of files.
Simulation modeling.

Q1 part B

Pipelining:

Pipelining enables a processor to work simultaneously on multiple instructions by performing a different phase for each of the multiple instructions at the same time.

Branch prediction:

Branch prediction potentially

increased the amount of work available for the processor to execute.

Branch prediction. superscalar execution: This is the ability to issue more than one instruction in every processor clock cycle. In effect, multiple parallel pipelines are used

Data flow analysis.

The processor analyzes which instructions are dependant on each other's results. or data to create an optimized schedule of instructions.

speculative execution:-

This enables the process or to keep its execution engines as busy as possible by executing instructions that are likely to be ~~needed~~. needed.

Q. part E

power:

As the density of logic and the clock speed on a chip increase, so the power density increases and also dissipated the heat.

RC delay:

The speed at which electrons can flow on a chip between transistors is limited by the resistance and capasitance of the metal wires connecting them; specifically, delay increases as the RC product increases.

Memory latency:

Memory access speed (latency) and transfer speed (through put) lag processor speed.

Q1 part (b)

The speed up using a parallel processor with N processors that fully exploits the parallel portion of the program is as follows.

speed up = Time to execute program on a single processor / time to execute program on N parallel procesor.

$= T(1-f) + TF/T(1-f) + Tf/N = 1(1-f) + f/N$

Q 1 E

Multicore:

* The Use of multiple processors on the same chip provides the potential to increase performance without increasing the clock rate.
* Strategy is to use two simpler processors on the chip rather than one more complex processor.
* With two processors larger cashes are justified.
* As cashes became larger it made performance sense to create two and then three levels of cashe on a chip.

MIC:

Leap in performance as well as the challenges in developing software to exploit such a larger number of cores.

The multicore and MIC strategy involves a homogeneous collection of general purpose processors on a single chip.

GPUS:-

* Core designed to perform parallel operations on graphics data.
* Traditionally found on a plug-in graphics card, it is used to encode and render 2D and 3D graphics as well as process video.
* Used as vector processors for a variety of applications that require repetitive computations.

Q2 A

Effective CPI:

$$CPi = (1 * 46000) + (2 * 33000) +$$

$$-(2 * 16000) + (2 * 9000) / 100$$

$$CPi = 162000 / 100$$

$$CPi = 1620$$

MiPS Rate:

MiPS rate = 60 MHZ / 1620 * 106

MiPS rate = 60 * 106 / 1620 * 106

MiPS rate = 60 / 1620

MiPS rate = 0.037

Execution Time:

T = IC / (MiPS * 106)

T = 104000 / (0.037 * 106)

T = 104000 / 37 * 103

T = 2811 * 10-3

T = 2.811 Sec

Q2 B

For machine A:-

CPI = (1*8 + 3*4 + 4*2 + 3*4) x 10^6 / (8+4+2+4) x 10^6

CPI = 40 x 10^6 / 18 x 10^6

CPI = 2.22

MIPS rate = 200 MHz / 2.22 x 10^6

MIPS rate = 200 x 10^6 / 2.22 x 10^6

MIPS rate = 90

T = Ic / (MIPS * 10^6)

T = 18 x 10^6 / 90 x 10^6

T = 0.2 sec

For Machine B:-

CPI = (1 x 10 + 2 x 8 + 4 x 2 + 3 x 4) x 10^6 / (10 + 8 + 2 + 4) x 10^6

CPI = 46 / 24

CPI = 1.92

MIPS rate = 200 MHz / 1.92 x 10^6

MIPS rate = 200 x 10^6 / 1.92 x 10^6

MIPS rate = 104

T = Ic / (MIPS x 10^6)

T = 24 x 10^6 / 104 x 10^6

T = 0.23 sec

Q2 C:-

The MIPS rate could be computed as the following:

MIPS rate = IC / T x 10^6

IC = MIPS rate x T x 10^6

By ratio

18 x 1x x 10^6 / 1 x 12x x 10^6

= 18/12

= 1.5

b:-

Regarding to the VAX 11/780, the

CPI = (5 MHz) / (1×10^6) = 5x 10^6 / 1 x 10^6

= 5/1 = 5

Regarding to the IBM RS/6000, the

CPI = (25 MHz) / (18×10^6) = 25 x 10^6 / 18 x 10^6

= 25/18 = 1.4

Q1 part D :-

A. Since we have the same instruction mix, that means the additional instructions for each task could be alloted appropriately between the instruction types. Therefore, the following table be gotten:

Instrudion type	CPI	Instruction Mix
Arithmetic and logic	1	60 %
Load/st are with cashe hit	2	18 %
Branch	4	12 %
Memory reference with cashe miss	12	10 %

The average CPi = (1x0.6) + (2x0.18) + (4x0.12) + (12x0.1) = 2.64 Therefore, The CPi has been increased Since The time For memory access is also in Creased.

b MiPS = 400/2.64 = 152. There is a corresponding drop in The MiPS rate.

C. The Speedup Factor equals To the ratio of The execution Times. The execution Time is calculated as The following: T = ic/(MiPS*10^6) For The one Processor, T1 = (2*10^6)/(178*10^6) = 11ms.

For The 8 Processors, each Processor executes 1/8 of the 2million instructions Plus The 25,000

T8 = 2*10^6 ÷ 8 + 0.025*10^6 / 152*10^6

T8 = 1.8 ms

Therefore we have

Speedup = Time To execute Program on a Single Processor/ Time To execute Program on N Parallel Processor

Speedup = 11/1.8

Speedup = 6.11

d. BY depending on The information given, It is not obvious how to quantify This EFFect in Amdahl's EQuation. Therefore, if it is Supposed that the FarcTion of code, which is parallelizable, is F = 1, Then Amdahl's Law decreases To

Speedup = N = 8.

Therefore, the actual Speedup is only about 75% of the Theoretical Speedup.