# DIGITAL LOGIC DESIGN

Final Assignment
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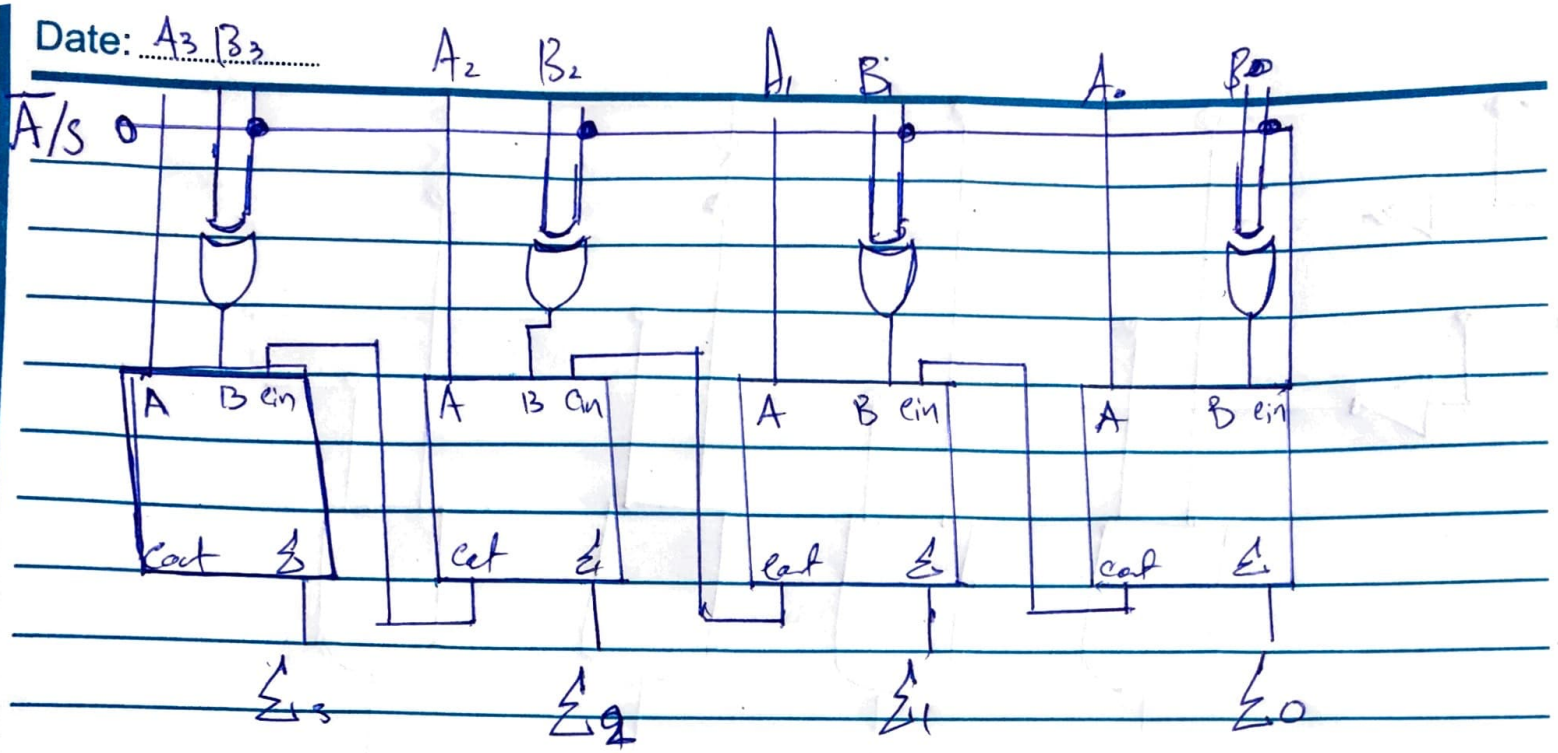
15453
Csc-201

Q.1 Draw and explain the logic diagram for each of the following:

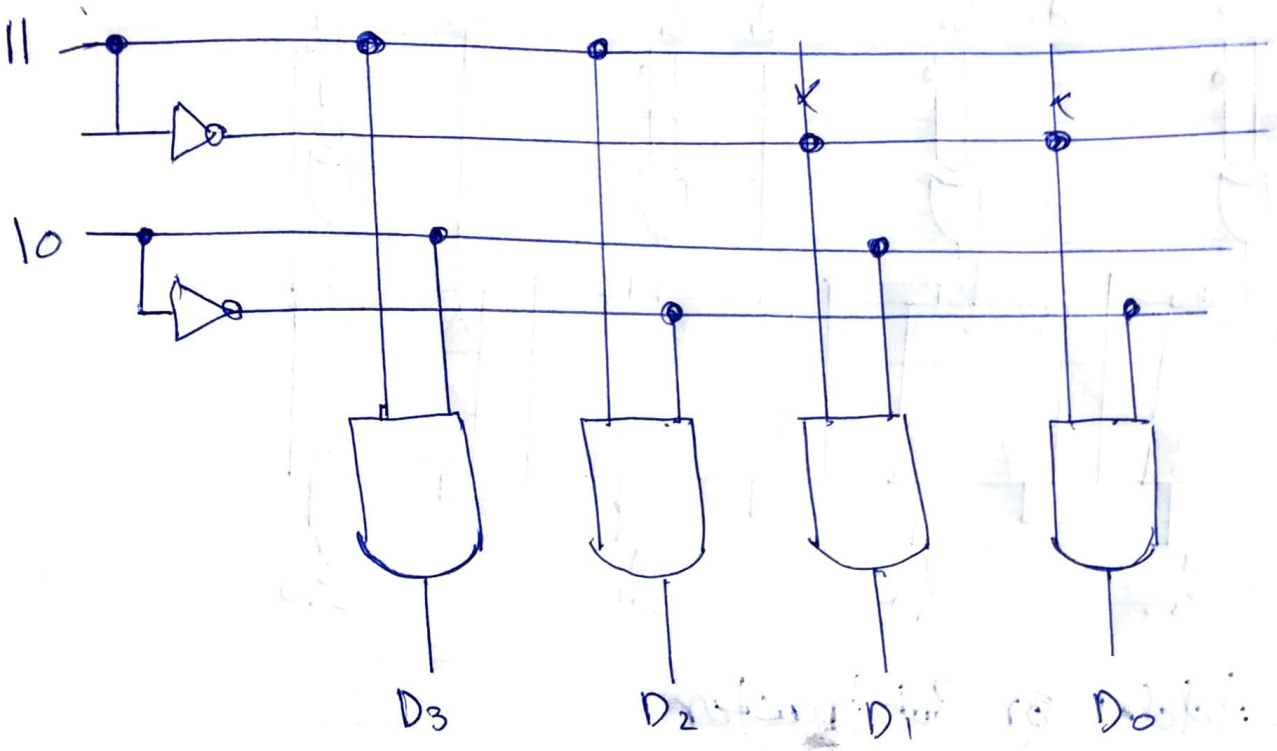
a) A circuit for adding or subtracting two 4-bit numbers




## 4bit Adder or Subtracter

The Circuit above is a 4bit adder or Subtracter that can add and subtract 4bit numbers in a form used in Computers. Positive number in true form, negative number in Complement form.

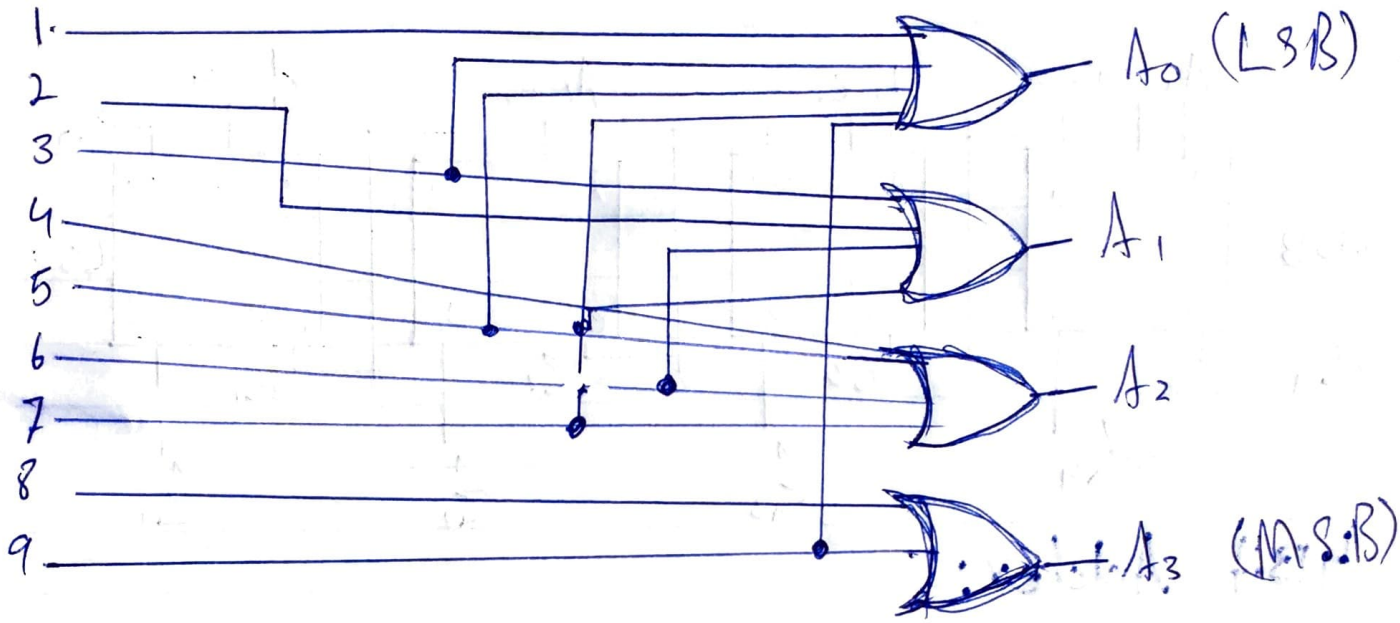
b) 4-bit active low decoder




## 4bit Active-Low Decoder:

Above is the circuitry for a 4 bit active low decoder. The input bits are decoded as they pass through the circuit and output is shown in the $D_3D_2D_1D_0$ form.

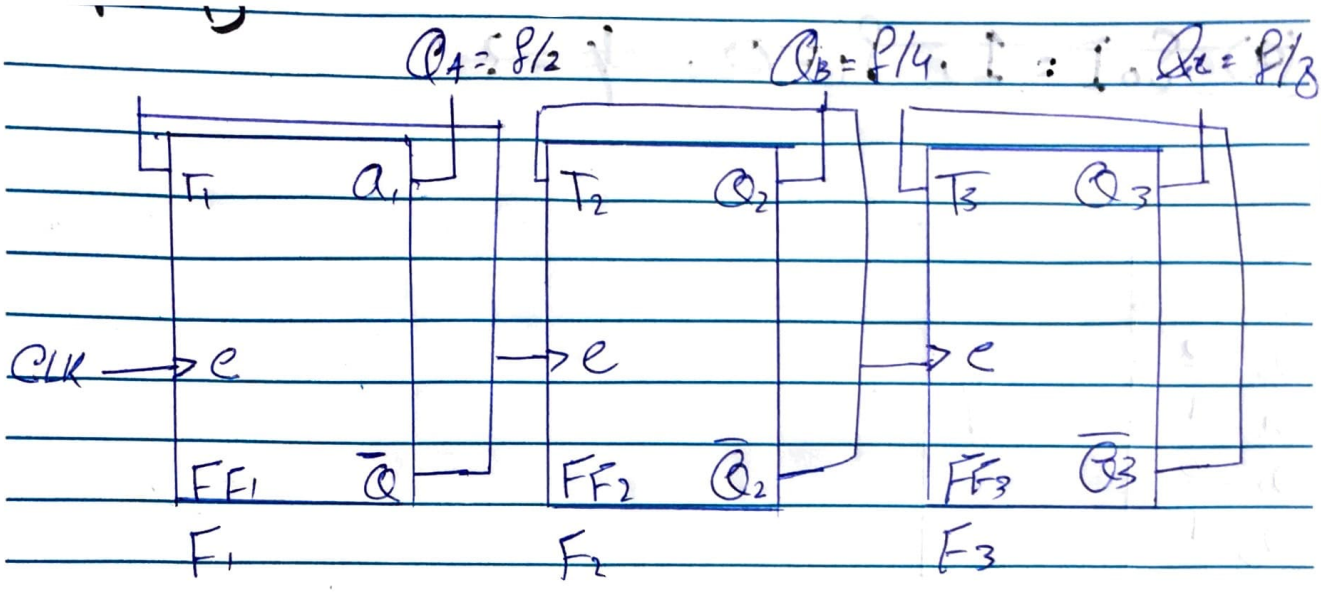
c) Decimal to BCD encoder




## Decimal to BCD Encoder:

Above is the logic circuit of a Decimal to BCD encoder.
When a Hight appears on one of the decimal digit input lines the appropriate levels occure on the four BCD output lines.

d) Frequency divider (Use 3 J-K flip-flops and assume 16 kHz frequency of the initial wave-form.)



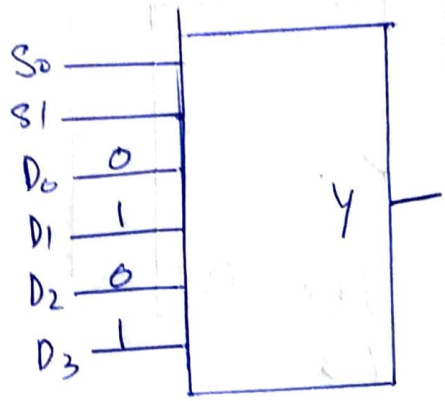

# Frequency Devider:

here if the input frequency is 16kHz then at given nodes the frequency will be:

$Q_A = f/2 = 16kHz/2 = 8kHz$
$Q_B = f/4 = 16kHz/4 = 4kHz$
$Q_C = f/8 = 16kHz/8 = 2kHz$

Q.2 For the 4-input multiplexer, data inputs are given as:
D0 =0,D1 =1,D2 =0,D3 =1
Find the output Y if the select inputs are given as:

a) S0 =1,S1 =0
b) S0 =0,S1 =1
c) S0 =1,S1 =1
d) S0 =0,S1 =0




(a) For $S_0 = 1$ and $S_1 = 0$,

$S_0 . S_1 = 10 \Rightarrow D_2$. hence $\boxed{Y = 0}$

(b) For $S_0 = 0$ and $S_1 = 1$,

$S_0 . S_1 = 01 \Rightarrow D_1$, hence $\boxed{Y = 1}$

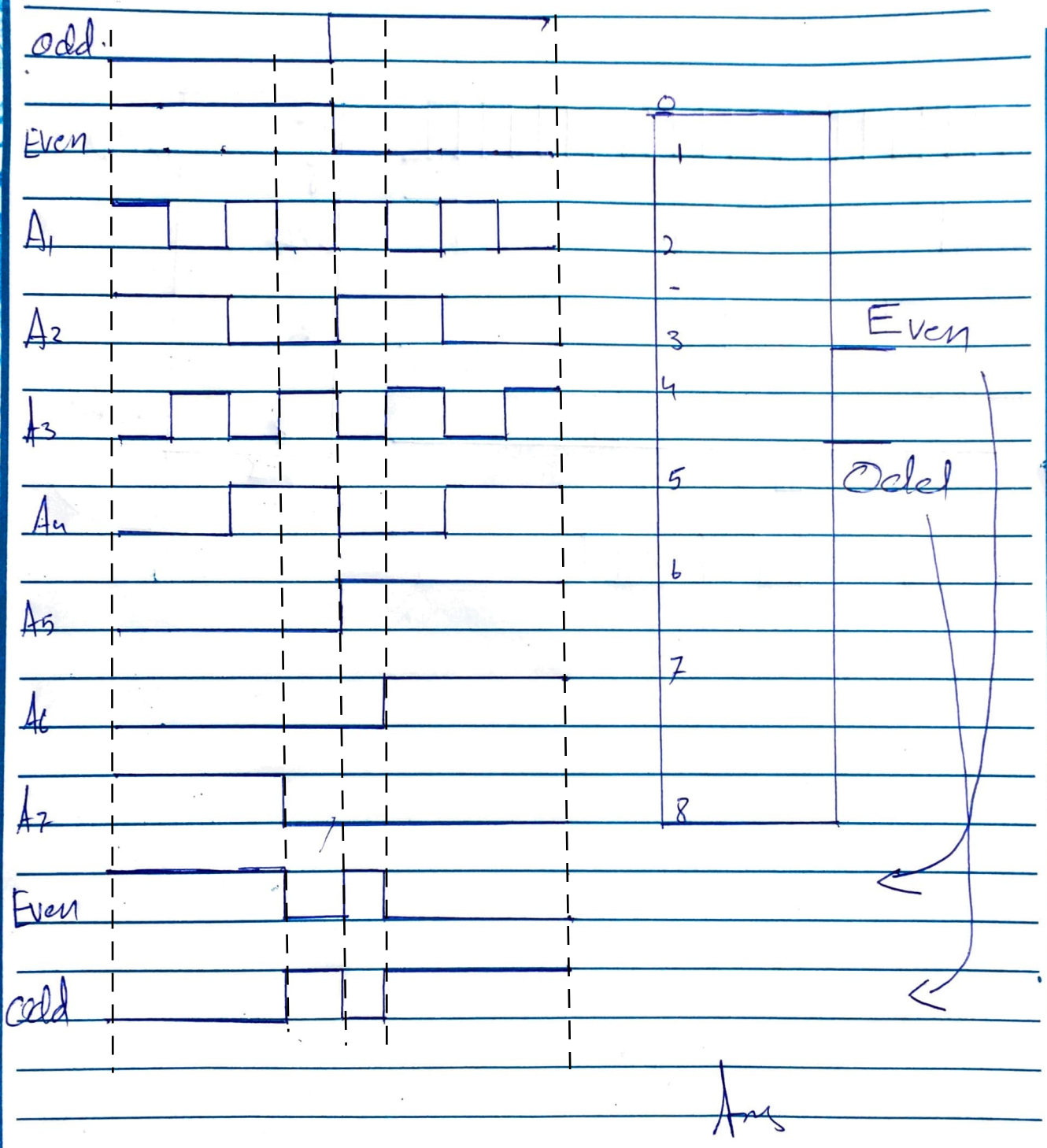
(c) For $S_1 = 1$ and $S_0 = 1$

$S_0 . S_1 = 11, \Rightarrow D_3$, hence $\boxed{Y = 1}$

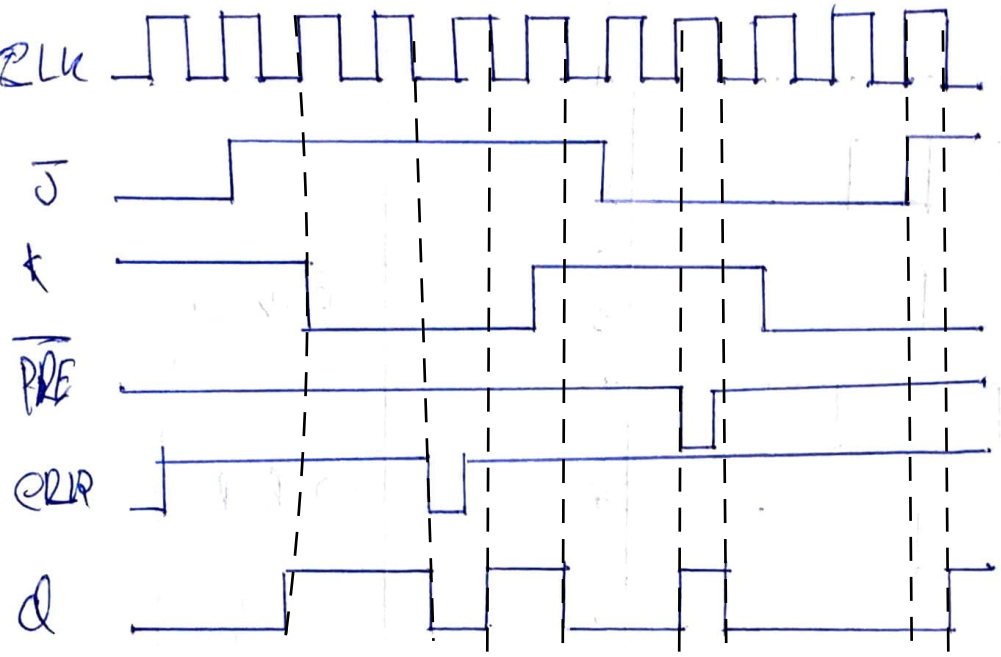
(d) For $S_0 = 0$ and $S_1 = 0$

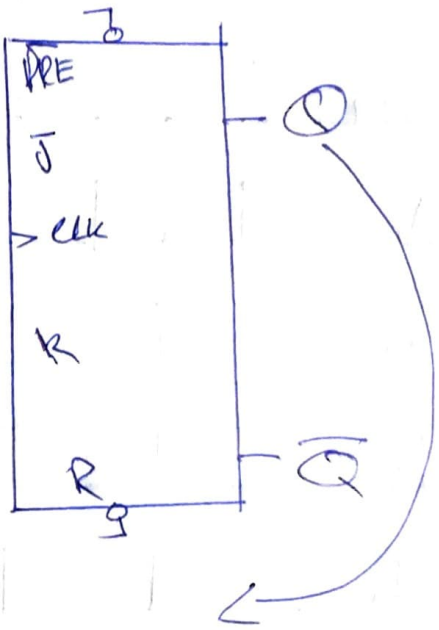
$S_0 . S_1 = 00 \Rightarrow D_0$, hence $\boxed{Y = 0}$

Q.3 Timing diagram in Figure 01 shows inputs to a 9-bit parity checker. Draw the ∑ Even and ∑ Odd output for the even parity checking.

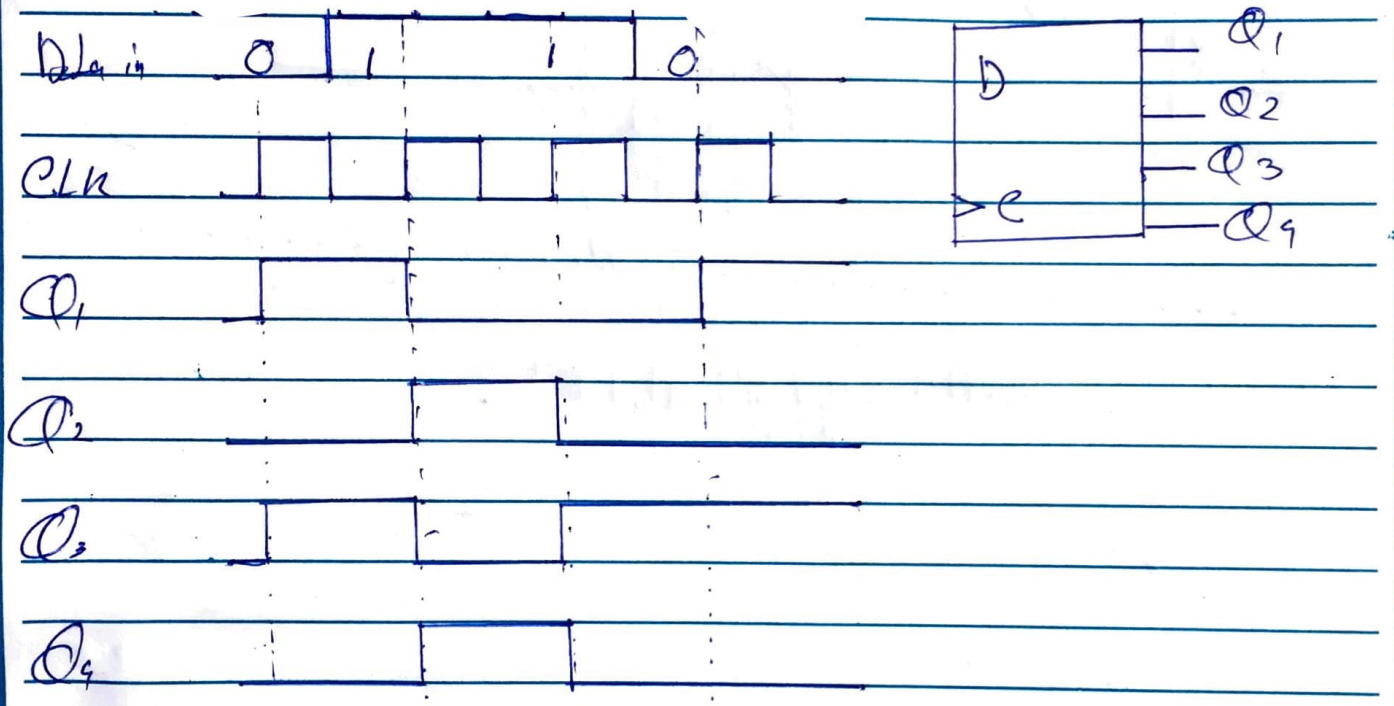


Q.4 The waveforms in Figure 02 are applied to the J, K, CLK, $PRE$, and $CLR$ inputs as indicated. Determine the Q output, if the flip-flop is initially RESET.

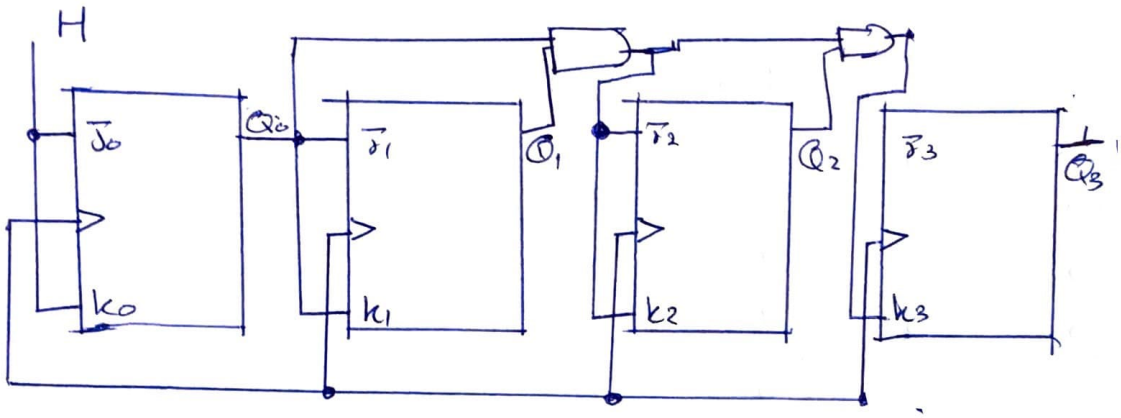


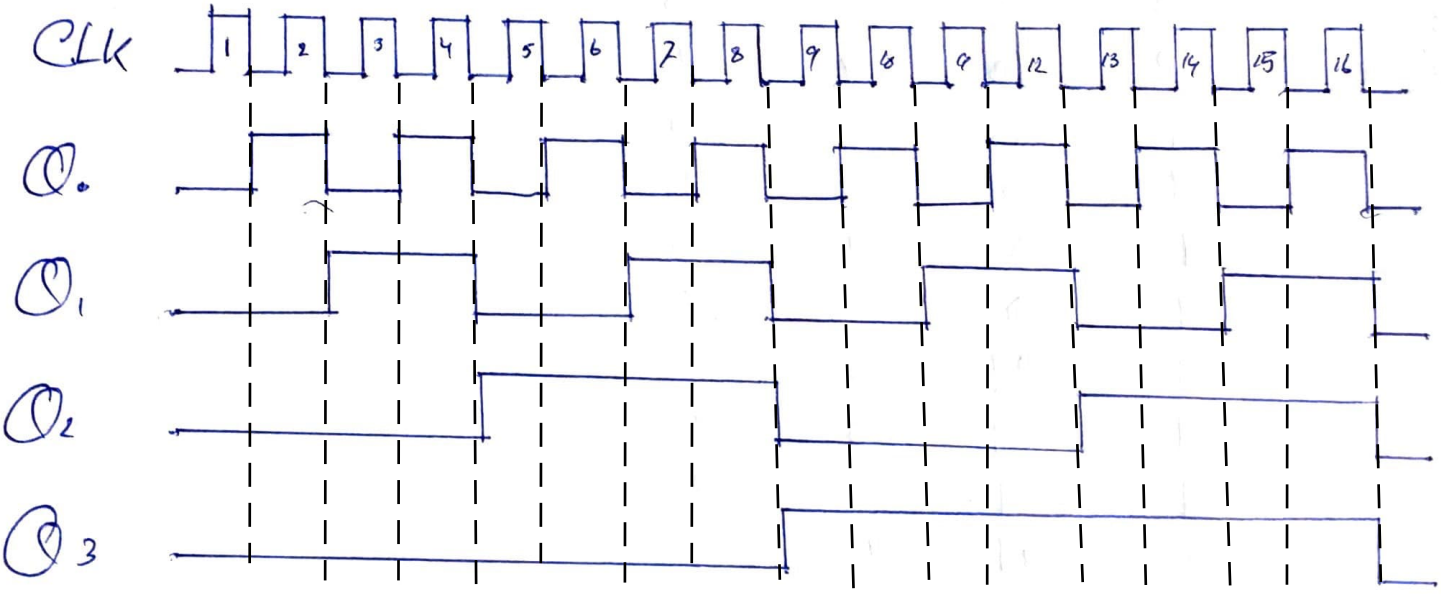



Q.5 Use the waveforms in Figure 03 to draw the timing diagram for the parallel outputs (Q1, Q2, Q3, Q4) for the shift register. Assume that register is initially cleared.



Q.6 Draw the logic diagram and timing diagram forthe 4-stage synchronous binary counter. Verify that the waveforms of the Q outputs represent the proper binary number after each clock pulse.



| CLK | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | |
|---|---|---|---|---|---|
| initially | 0 | 0 | 0 | 0 | |
| 1 | 0 | 0 | 0 | 1 | |
| 2 | 0 | 0 | 1 | 0 | |
| 3 | 0 | 0 | 1 | 1 | |
| 4 | 0 | 1 | 0 | 0 | |
| 5 | 0 | 1 | 0 | 1 | |
| 6 | 0 | 1 | 1 | 0 | |
| 7 | 0 | 1 | 1 | 1 | |
| 8 | 1 | 0 | 0 | 0 | |
| 9 | 1 | 0 | 0 | 1 | |
| 10 | 1 | 0 | 1 | 0 | |
| 11 | 1 | 0 | 1 | 1 | |
| 12 | 1 | 1 | 0 | 0 | |
| 13 | 1 | 1 | 0 | 1 | |
| 14 | 1 | 1 | 1 | 0 | |
| 15 | 1 | 1 | 1 | 1 | |
| 16 | 0 | 0 | 0 | 0 | Reset |