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Subject # Computer Architecture.

Assignment # 02 final term.

Department # Computer Science.

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Q No 1 Give answer to each of the following.

(a)

Addressable unit :-

In some addressable unit is the word, However many systems allow addressing at byte level = In any case. $2^A = N$

Unit of transfer :-

For main memory This is the number of bits read out of or written into memory at a time. The unit of transfer not equal a word or an addressable unit.

Word :- The natural unit of organization

of memory. The size of the word is typically equal to the number of bits used to represent an integer and to the instruction length.

Q No 1

(b)

Ans Probably the most effective at least recently used (LRU) replace that block in the set that has been in the cache longest with no reference to it. For two way associative line include a use bit. When a line is referenced, its use bit is set to 1 and the use bit of other line that set to 0, Use bit of the other line in that set is set to 0.
When a block is to be read into the set, The line those line use bit is 0. is used. Because we are assuming that more recently used memory location are more likely to be referenced. LRU should give the best hit ratio LRU is also relatively easy to implement for a fully associative cache.
The cache mechanism maintains a separate list of indexes all the lines in the cache. When a line is referenced in it move the front of the list for replacement the line at

the back of the list is used.
Because of its simplicity of implementation LRU is the most popular replacement algorithm. Still another possibility is at least frequently used (LFU) replace that block in the set that has expressed the fewest references. LFU could be implemented by associating a counter with each line.
A technique not based on usag, not LRU, LFU, FIFO or some varient is to pick a line at random from among the candidate lines. Simulation studies have shown that random replacement provides only slightly inferior performance to an algorithm based on usag.

Q No 1 :

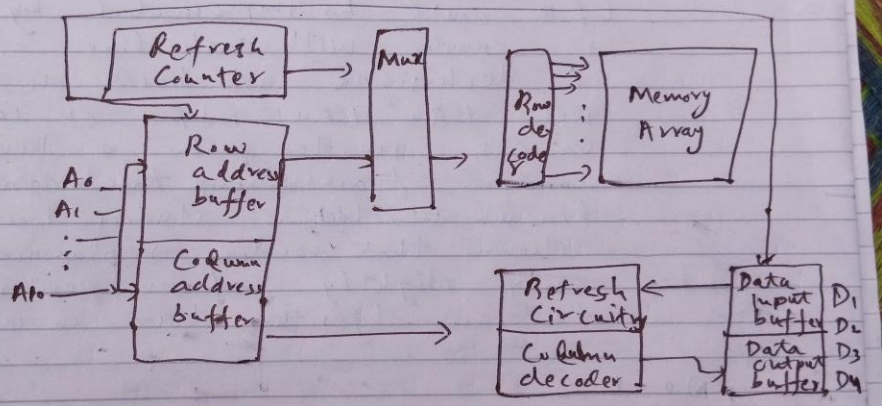
(c)

Ans The SRAM address line is used to open or closed a switch. The address line control two transistor (T_5 and T_6). When a signal is applied this line the two transistors are switched on allowing on read or write operation for a write operation the desired bit value is applied to line B. This forces the four transistors (T_1, T_2, T_3, T_4) into the proper state

For a read operation. The bit value is read from line B.

Q No. 1

(d)



Because of only four bits are read/write to this DRAM. there must be multiple DRAMs connected to the memory controller to read/write a word of data to the bus. All the DRAMs require a refresh operation. A simple technique for refreshing is in effect to disable the DRAM.

Q No 1

(e)

Ans Bits are produce move closely on DVD. The spacing b/w loops of a spiral on a CD is 1.6 μm and minimum distance b/w bits along spiral is 0.834 μm.

The DVD uses a layer with shorter wavelength and actives a loop spacing of 0.7 μm and a minimum distance b/w bits of 0.4 μm. The result of these two improvements is about a seven fold increase in capacity to about 4.7 GB.

(2) The DVD employer a second layer of bits and lands on the top of the reflective layer and by adjusting focus, the passes in DVD drives can read each layer separately.

This technique almost doubles the capacity of this disk to about 8.5 GB.

The lower reflectively of the second layer limits, its storage capacity so, that a full doubling is not achieved

(3) The DVD ROM can be two sides whereas data are recorded on only one side of CD.

This brings total capacity up to 17 GB.

Q No 2 Differentiate each of the following in detail?

(a)

Ans EEPROM and Flash memory:-

Flash memory is the one kind of Non-volatile random access memory. It is slower than RAM but faster than hard drives. The main difference b/w EEPROM and flash memory is that most EEPROM devices can erase any byte of memory at any time. Flash memory can only erase an entire chunk or sector of memory at a time flash memory is used primarily for storage while RAM performs calculations on the data retrieved from storage, By their nature, flash memory and Ram are faster than storage alternatives, such as hard-disk and tape. In term of flash memory

Q No 2

(b)

Ans In this content hard failure are errors that occure through process defects and/or circuit bugs. hard failure or repeatable with the correct sequence of actions with in the micro-controller soft error occurs through

no failure of the circuit or defect but due to an external source that causes the data change.

Q No 2

(c)

Ans Disk read/write heads are the small parts of a disk drive which move above the disk platter and transform the platters magnetic field into electrical current or read me disk vice virca. transform electrical current into magnectic field.

Q No 2

(d)

Ans Parallel Access Raid:-

In a parallel access array all members disk participate in the execution of every I/O request typically. The spindles of the individuals drives are synchronized so that each disk hand is an in the same position on each disk at any given time.

As in the other RAID schemes data striping is used. In the case of Raid 2 and 3 the strips are very small often as small as a single

are very byte or word.

Independent Access Raid:-

In independent access array each member disks operation independently, so that separate I/O requests can be satisfied in parallel. Because of this independent access arrays are more suitable for application that require a high data data transfer rates. As in the other Raid schemes data stripping is used. In the case of Raid 4 through 6. This strips are relatively large.

Q No 2

(E)

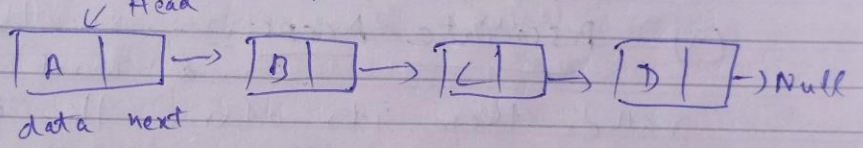
Ans 2 Blue ray and HD DVD both uses a blue laser which has a shorter wavelength than read ones. In contrast HD DVDs can hold 25 GB on one layer Even more can be paked into blue ray / HD DVD disks if they use more than one layer one side of the disk.

Q No 3 Write note on each of the following

(a) Memory Access Methods?

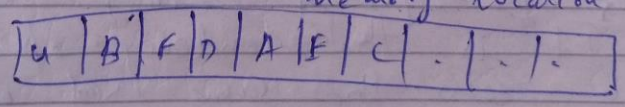
(1) Sequential Access

In this method, the memory is accessed in a specific linear sequential manners like accessing in a single linked list.
Application of the sequential access memory are magnetic tapes, magnetic disks and optical memories.



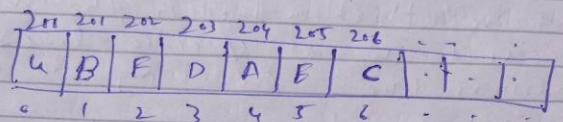
(2) Random Access:-

In this method any location of the memory can be accessed randomly like accessing in array Physical location are independent in this access method.
Application of this method access are RAM and ROM.



(3) Direct Access: In this method the particular location of the memory can be accessed directly like

accessing in array. This method is a combination of above two access methods. The access time depends on the memory organization and characteristics of storage technology. The access is semi-random or direct.



Application of this direct access memory is magnetic hard disk read/write header.

(4) **Associate Access:-** In this memory, a word is accessed rather then its address. This access method is a spacial time of random access method Applicatim of this direct memory access is cache memory.

Q No 3

(b) **Principles of locality:-** In Computer Science locality of reference also known as principle of locality.

(1) It is the tendency of processor to access the same set of memory location repetitively over a short period of time.

(2) There are two basic types of reference locality temporal and spatial locality

(3) Refers to use of data elements within a relatively small elements within relatively close storage, location sequential locality occurs when data elements are arranged and accessed linearly such as traversing the elements in one dimensional array.

Q No 3

(c)

In computer architecture, cache coherence is the uniformly of shared resources data that ends up stored in multiple local caches. When clients in a system maintain caches of a common memory resources, problems may rise with incoherent data which is particularly the case with CPUs with a multiprocessing system. In the illustration in the right consider both the clients have a cached copy of a particular block from a previous read; suppose the client on the button on the top could be left within an invalid cache of memory without any notification of the change cache coherence is intended to manage such conflicts by maintaining a coherent view of the data values in multiple caches.

Q No 3

(d)

Ans There are two practical issues peculiar to SSDs that are not faced by HDDs SSD performance has a tendency to slow down as the device is used.

→ The entire block must be read from the flash memory and placed in a RAM buffer.

→ Before the block can be written back to flash memory

→ Flash memory become unusable after a certain number of writes.

→ Using Wear leveling algorithms that evenly distributes write accross block of cells.

Bad – block management techniques most flash-devices estimate their own remaining lifetimes so system can participate failure and take preemptive action.

Q No 3

(E) Discuss CD read and write?

Ans Read:

Information are retrieved from CD or CD-Rom. by a low powerd lases house in an optical disk player or drive unit. The laser shines through the clear poly carbonate while a motor spins the disk part it. The intensity

of the right reflected of the laser changes as it encounter a bit. Specifically if the laser beams falls on a bit which has a some what rough surface the light scatters and a low intensity is reflected back to source. The area b/w bits are called lands. A land is a smooth surface which reflects back at higher intensity. The change b/w lands and bits is detected by a photo sensor and converted into a digital signal. The sensor tests the surface at regular intervals. The beginning or ends of a bit represent a 0,1. When no change in occurs between intervals a = 0 is recorded.

Write:-

Recall that on a megnetic disk information is recorded in concentration with the simplest constant angular velocity (car). The number of bits per tracke constant. An increase in density is achieved with multiple zoned recording. In which the surface is divided into a number of zones, with zones further from the cortex containing more bits than zones closer to the cortex

Although this techniques increases capacity. It is still not optional.

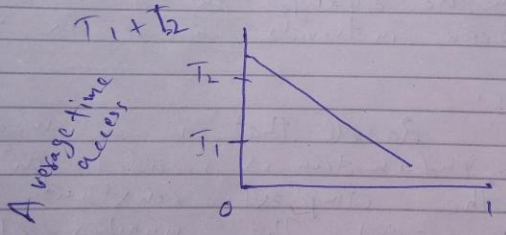
Q No 4 Solve each of the following?

(a)

Ans Suppose 95% of the memory access are found in level 1 then the average time to access a word can be expressed as

$(0.95)(0.01\mu s) + (0.05)(0.01\mu s) + (0.1\mu s)$
$= 0.0095 + 0.0005 = 0.015\ \mu s.$

The average access time is much closer to 0.01 μs than 0.1 μs as desired.



Q No 4

(b)

Total block in the cache = 2k bytes / 16 bytes $= 2^3 \times 2^{10} / 2^4$
$= 2^9 = 512$

number of sets = number of blocks in cache / 2
$= 512/2 = 256$
number of set in cache $= 2^8$

size block = 16 = 2^4

Size of memory = $2^6 \times 2^{20} = 2^{26}$

type size of memory = set size of block

Tag = Size of memory − set − size of block

Tag. = 26 − 8 − 4

Tag = 14

Tag	set	Size of block
14	8	4

Ans

Q No. 4

(d)

Ans 7200 revolution in 60 sec

1 revolution is 60/7200 or.

1 revolution conveying one entire track = 500 sector

500 sector = 6 ms

1 sector = 8 micro second

Now these 2 right things

(1) 2500 sector so time → 2500 × 8 ms
= 20 ms

(2) 1.28 MB = 1342177.28 bytes or
2621.44 sectors.
2622 sectors = 20.97 ms.

total time case.

Case (1) 4 + 2 + 20 = 26 ms

Case (2) 4 + 2 + 20.97 = 26.97 ms.

Q No 4

(a)

Suppose an 8-bit data word stored in memory is 10101010. Using the hamming edge determine what check bit would be stored in memory with the data word.

$m = 8$

$2^k - 1 >= k + m$

$2^4 - 1 >= 4 + 8$

$15 >= 12$

1	2	3	4	5	6	7	8	9	10	11	12
1	0	1	1	1	0	0	1	0	0	1	0

→ The check bit in a bit number 1, 2, 4, 4, 8

→ Check bit 8 calculated by values in bit number 9, 10, 11, and 12

→ Check bit 4 calculated by values in bit number 5, 6, 7 and 12

→ Check bit 2 calculated by values in bit number 3, 6, 7, 10 and 11

→ Check bit 1 calculated by values in bit number 3, 5, 7, 9, 10 and 11

→ Thus check bit are 1011.