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14127
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DLD

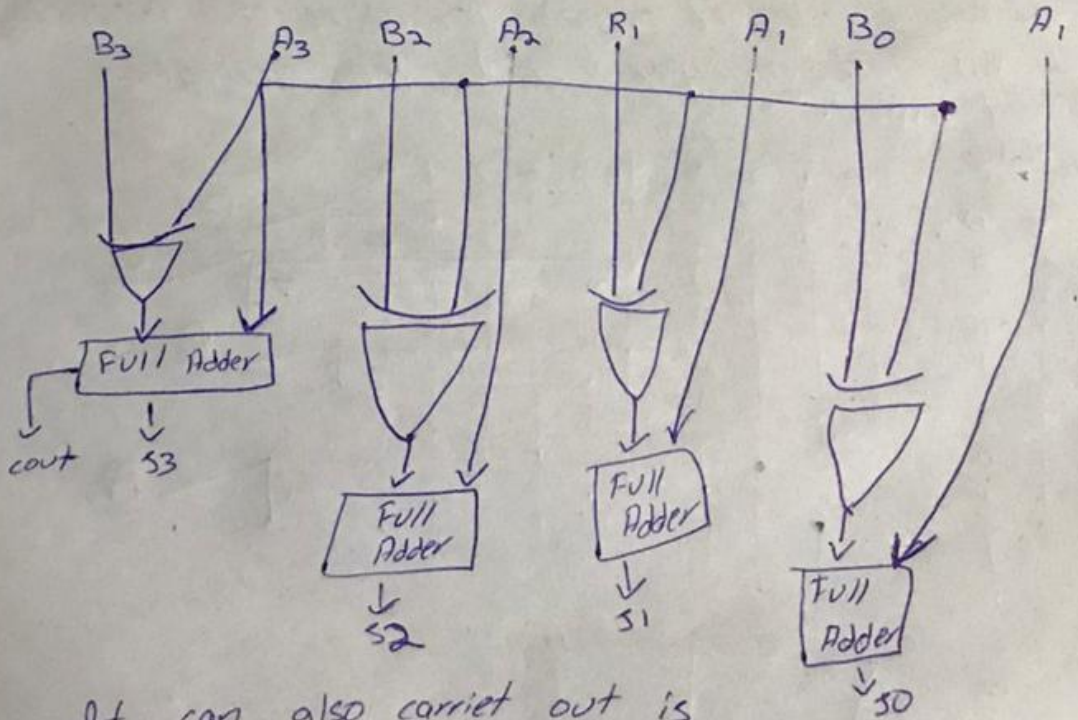
Q1 Answers

a) In digital circuits, A binary Adder-subtractor is one which is capable for both addition and subtraction of binary numbers in one circuit itself.
lets concider two 4-bit binary numbers A and B as inputs to the Digital Circuit for the operation with digits

A_0 A_1 A_2 A_3 for A
B_0 B_1 B_2 B_3 for B

It continues and full adder performing on 4-bit numbers, There is control line K that holds a binary value 0 or 1, which determines operation carried out in addition or subtraction.

Diagram:-

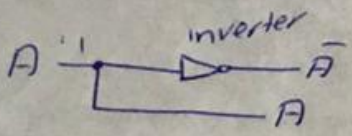


It can also carriet out is addition or subtraction.

Q1 (b) Answer:-

On digital circuits when a signal is "active low" means that the signal will performing its function when its logic level is 0, if it is anactive- low pin, you must pull that pin low by connecting it to ground. For an active high pin you connect it to your High voltage (usually 3.3V/5V)

4 bit depends upon the number of date inputs lines, so decoder that has a set of two or more bits will be defined as n-bit code. by ~~2~~ 2^n possibles values into a non binary one by setting exactly one of its n outputs to logic 1. If a binary decodes recieves n inputs it activates one and only one of its 2^n outputs based on that input with all ~~inputs~~ outputs deactivated.

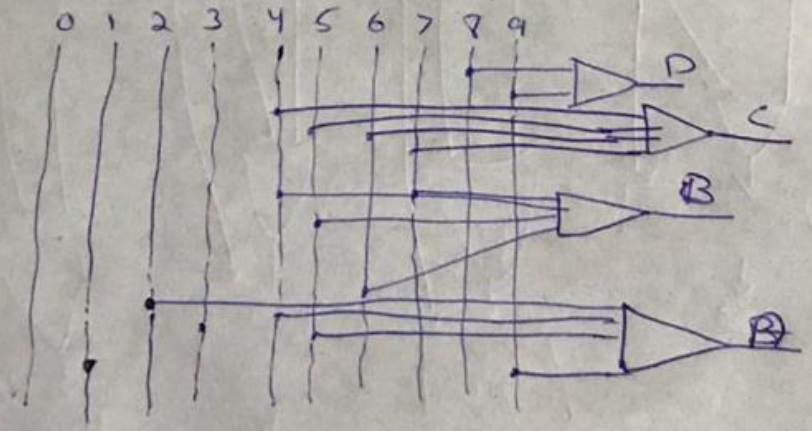


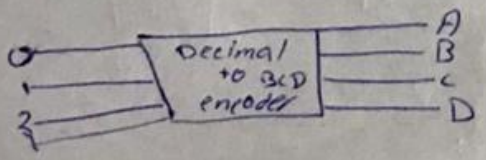
Q1 (c) Answer 1- Decimal to BCD encoder

A decimal to BCD encoder is also known as 10-line to 4-line encoder. It accepts 10-inputs and produces a 4-bit out corresponding to the activated decimal input.

Truth Table

0	D	C	B	A
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	0	0	1	1
5	0	1	0	0
6	0	1	0	1
7	0	1	1	0
8	0	1	1	1
9	1	0	0	0
	1	0	0	1





Q1 D Answer

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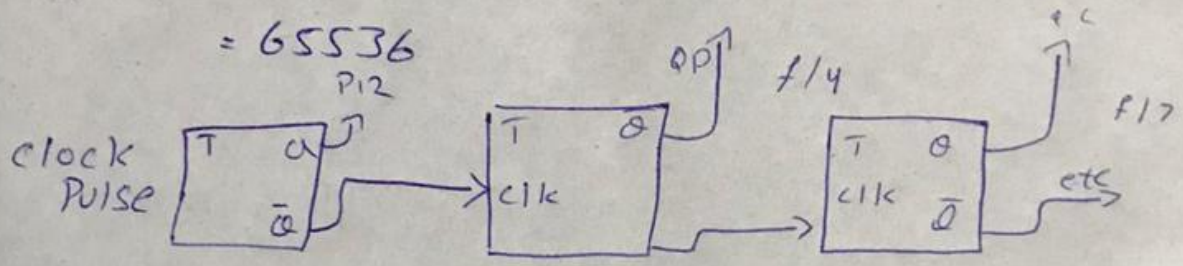
Frequency Divider

MoD $= 2^n$

$= 2^{16}$

$= 65536$



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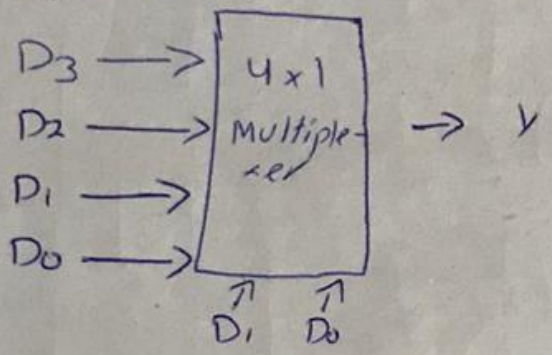
Q2 Answer

Sol:- Given inputs:-

$D_0 = 0$, $D_1 = 1$, $D_2 = 0$, $D_3 = 1$

4 x 1 Multiplexer has four data inputs D_0, D_1, D_2, D_2 two section lines S_1 and S_0 and one output y. The Block diagram.

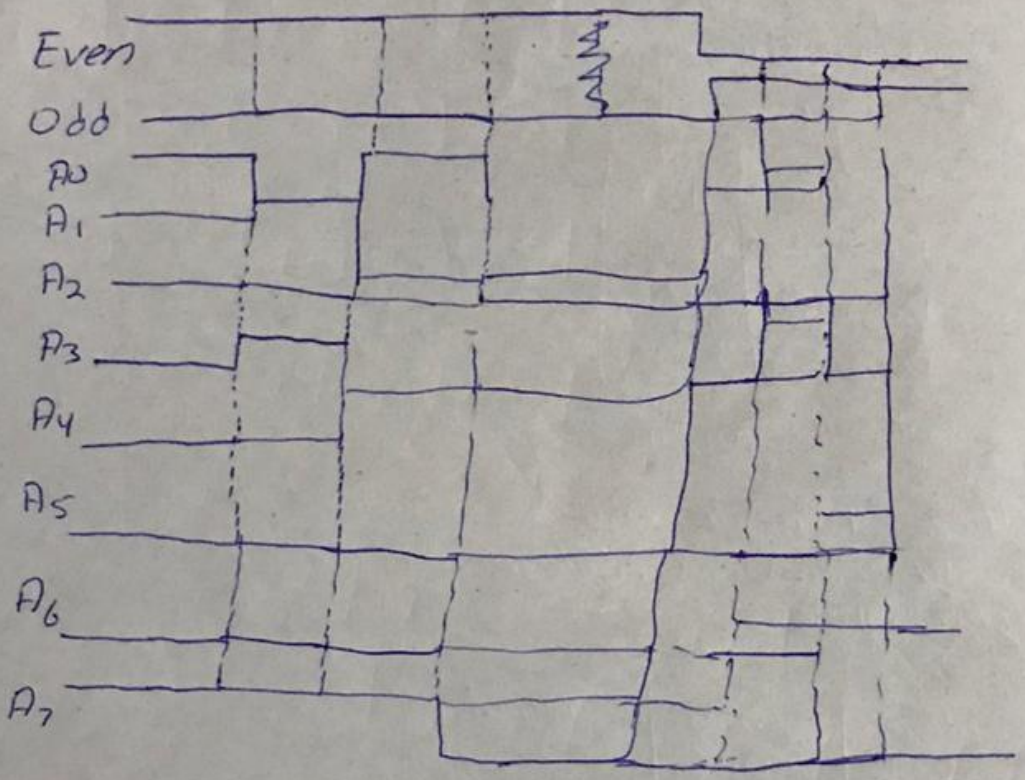


one of these 4 inputs will be connected to the output based on the combination of inputs present, at these two section, lines.

Section	Lines	Output
D_1	D_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

$Y = S_1 S_0' D_0 + S_1 S_0 D_1 + S_1 S_0' D_2 + S_1 S_0 D_3$ Ans.

Q3 Answer



(a) Even parity : 110100
(b) Even parity : 001100011
(c)

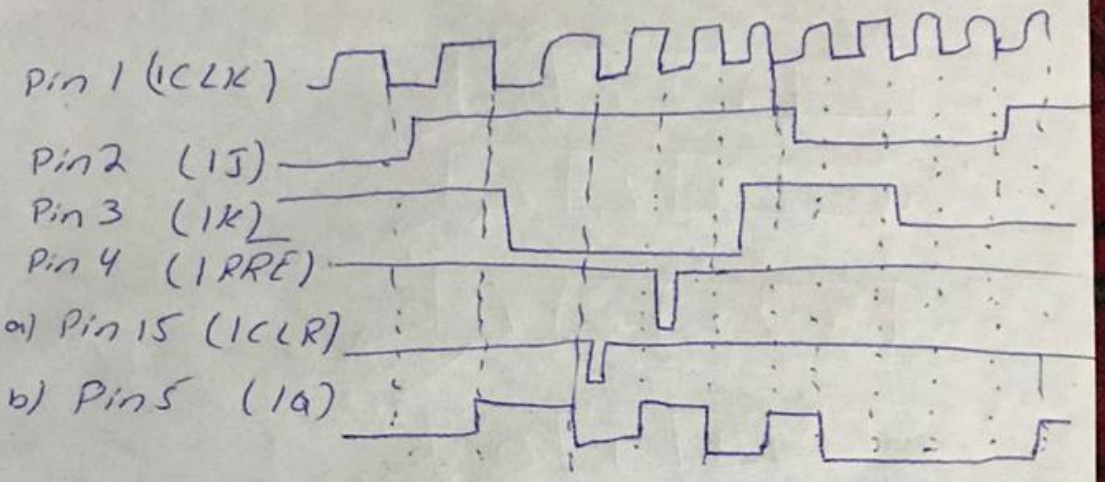
Generators / checkers.

(a) Even parity : 110100
(a) Odd parity : 11010101
A) Code is correct, four 1s

(b) Even parity : 001100011
(b) Odd parity : 11000001
(b) Code is error, seven 1s.

Q4 Answer. (6)

Soln The 1J, 1K, 1CLK, $1\overline{PRE}$ and $1\overline{CLR}$ waveforms are applied to one of the negative edge-triggered flip-flops in a 74HC112 package. Determine the 1Q output waveform.

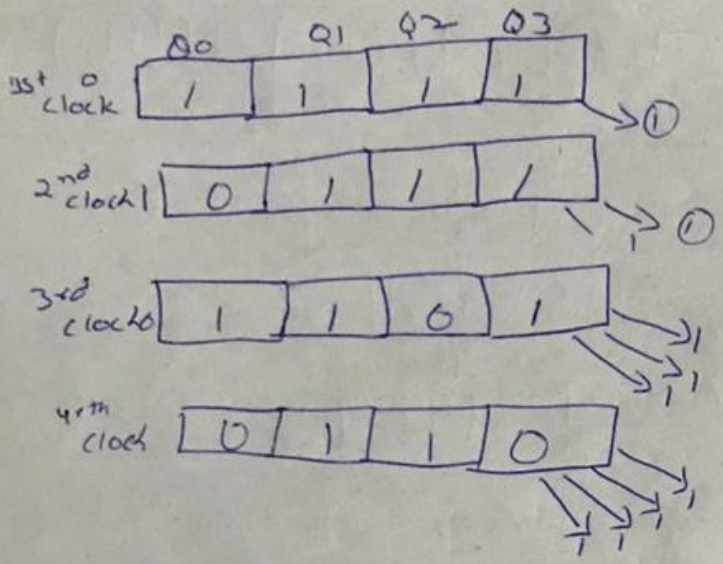


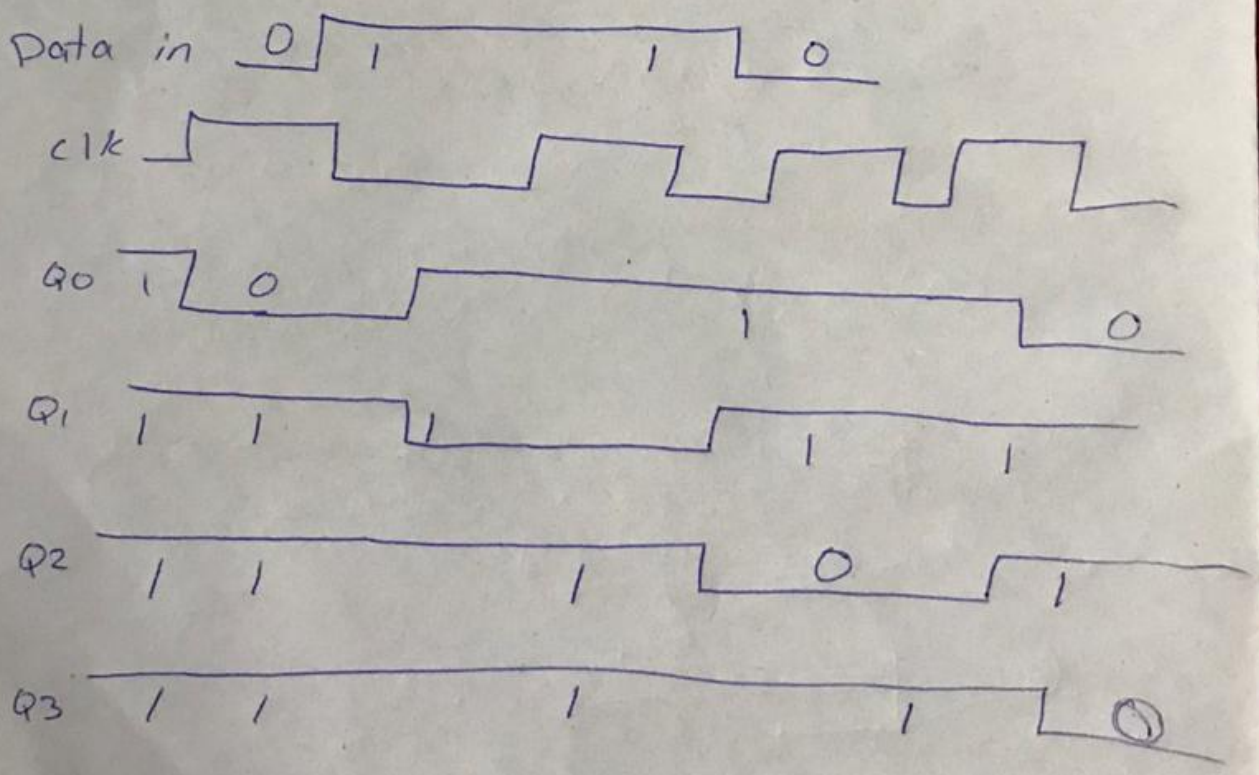
Solution:- The resulting 1Q waveform each time a low is applied to the $1\overline{PRE}$ or $1\overline{CLR}$, the flip-flop is set or reset regardless of the states of the other inputs.

Q5 Answer:-

Use the wave form.

Soln:-





Q6 Answer :-

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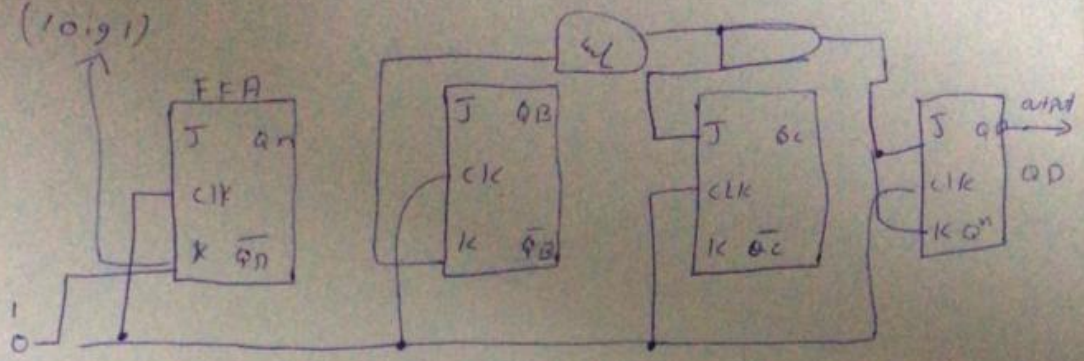

It can be seen above, that the external clock pulses are fed directly to each of the J-K flip flops in the counter chain, J and K inputs are all tied together in toggle mode. First flip-flop, flip-flop FFA (LSD) are they connected High, logic I allowing the flip-flop to toggle on every clock pilot. The J and K inputs of flip flop FFB are connected directly to the output QA of flip-flop FFA)

If we enable each JK flip wether or not all proceeding High we can obtain the same counting sequence.