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Class BS - SE - B

Subject DLD

8th Semester

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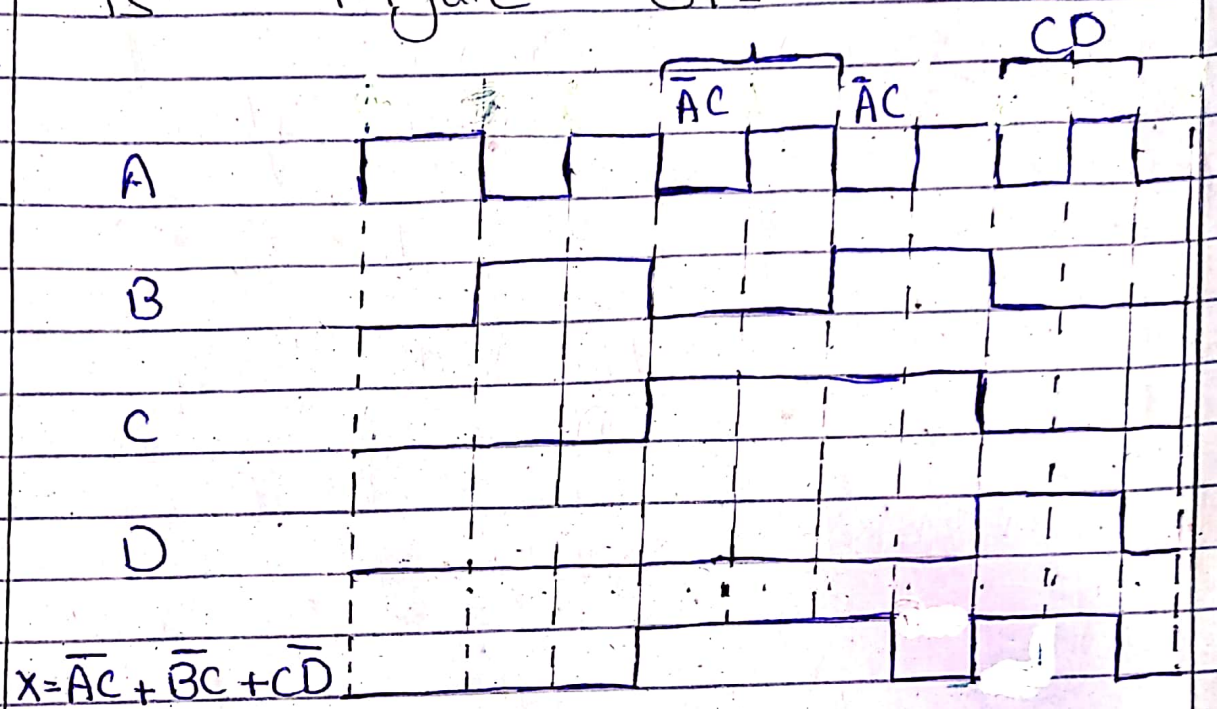
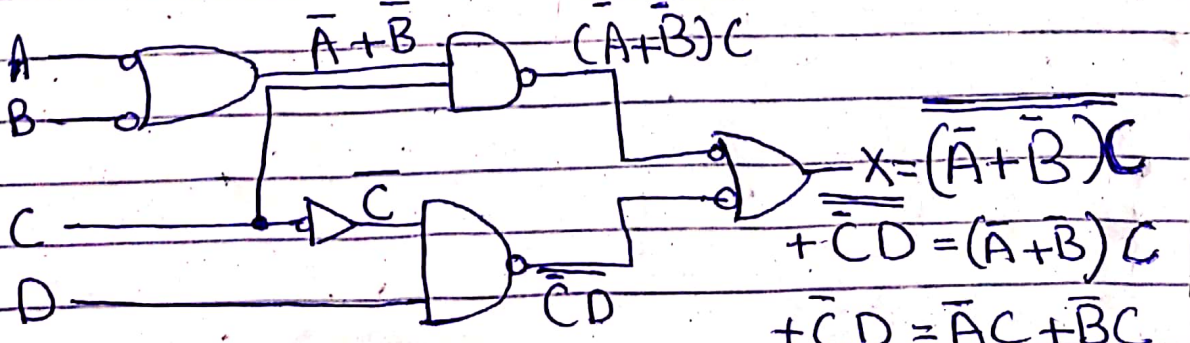
Q1:- Draw the logic circuit using the input (A, B, C, D) and output (X) waveform is Figure 01-

Ans:-



Sol:-

The output expression for the circuit is develop in The SOP from indicates that output is HIGH when A is LOW and C is HIGH or when B is LOW and C is HIGH or when C is LOW and D is HIGH-



Q2. For the 4-input multiplexer data input are given as, $D_0 = 0$, $D_1 = 1$, $D_2 = 0$, $D_3 = 1$

Ans 2

Data Select inputs		
S_1	S_0	input Selected
0	1	D_0
1	0	D_1
1	1	D_2
0	0	D_3

look at logical circuit required to perform this multiplexing operation. The data output is equal to the state of selected data input. You can therefore, derive a logic expression for output in terms of data input and the select inputs.

⇒ The data output is equal to D_0 only if $S_1 = 0$ and $S_0 = 1$: $Y = D_0 \bar{S}_1 \bar{S}_0$.

⇒ The data output is equal to D_1 only if $S_1 = 1$ and $S_0 = 0$: $Y = D_1 \bar{S}_1 S_0$

⇒ The data output is equal to D_2 only if $S_1 = 1$ and $S_0 = 1$: $Y = D_2 S_1 S_0$.

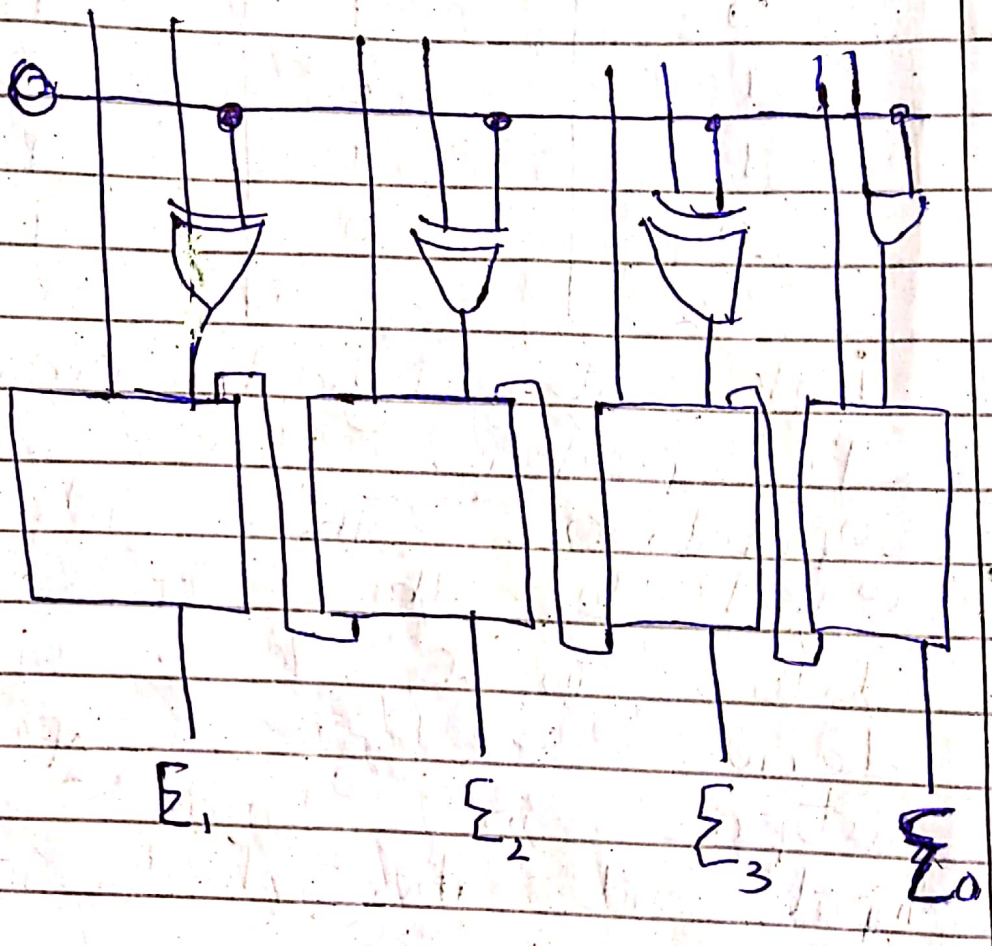
⇒ The data output is equal to D_3 only if $S_1 = 0$ and $S_0 = 0$ $Y = D_3 \bar{S}_1 \bar{S}_0$.

When these terms are ORed, the total expression for data output is

$$Y = D_0 \bar{S}_1 \bar{S}_0 + D_1 \bar{S}_1 S_0 + D_2 S_1 \bar{S}_0 + D_3 S_1 S_0$$

Q3. For the circuit in figure 02 assume the inputs are Add/Subt = 1, A = 1010 and B = 1101 what is output?

Ans: 3

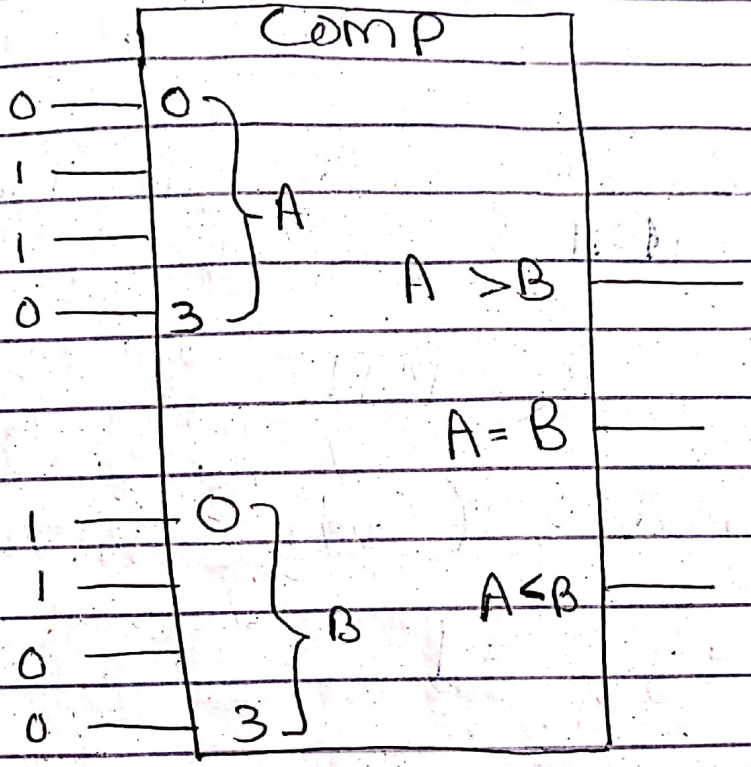


The Answer is

1 0 0 1

Q4/ Determine A=B, A>B, A<B output for the input member shown on the comparator in figure 6-22

Ans/4



Sol/

The number on the A inputs is 0110 and the number on B input is 0011. The A > B output is HIGH and the other output is LOW.

Q5 Show the logical required to convert a 4 bit Gray code to binary and use the logic to convert the follow Gray code word to binary : 1011

Ans 5

Sol:-

Convert Gray code to binary code = 1011

Gray code 1011

Method-1 : (Gray code to Binary)

$b_3 = g_3 = 1$

$b_2 = b_3 \oplus g_2 = 1 \oplus 0 = 1$

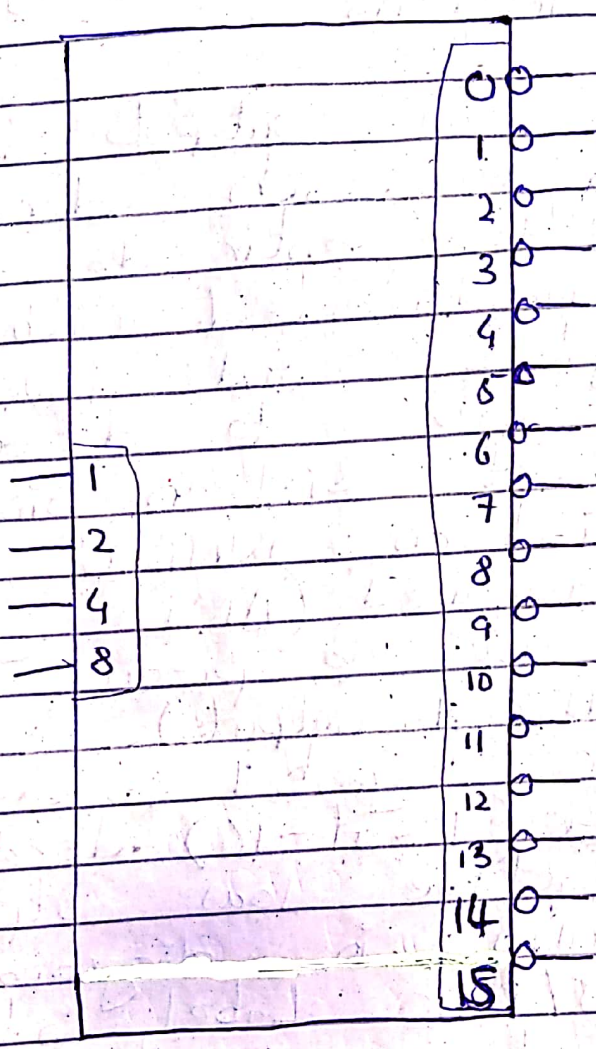
$b_1 = b_2 \oplus g_1 = 1 \oplus 1 = 0$

$b_0 = b_1 \oplus g_0 = 0 \oplus 1 = 1$

Binary Code : 1101

Q6. Draw and explain the logic diagram 4 bit active low decoder. (6)

Ans: 4 Bit Active decoder



The 4 Bit decorder to decode all positive combination of four bits, sixteen decoding gates are = 16). This type of decoder is commonly called either a 4-line-to-16-line decorder because there are four inputs and sixteen outputs or a 1-of-16 decorder because for any given code on the inputs, one of the sixteen outputs is activated.

A list of sixteen binary code and their corresponding decoding functions is give in diagram.

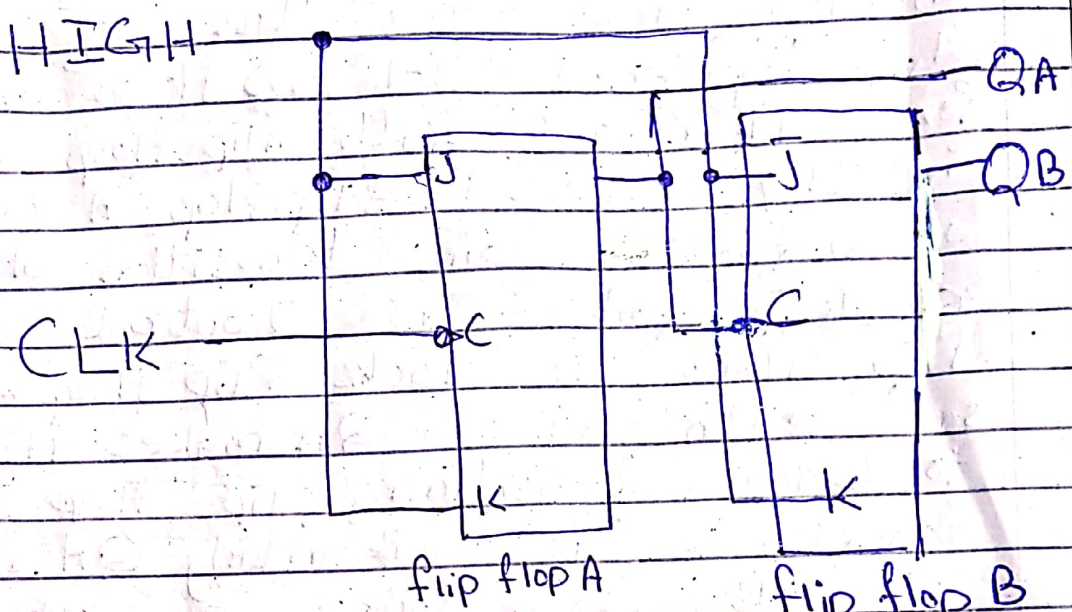
If an low output is required for each decoded number, the entir decorder can be implemented with NAND gates and inverters. In order to decode each of sixteen binary code, sixteen NAND gates are required (AND gates can be use to produce active - HIGH outputs).

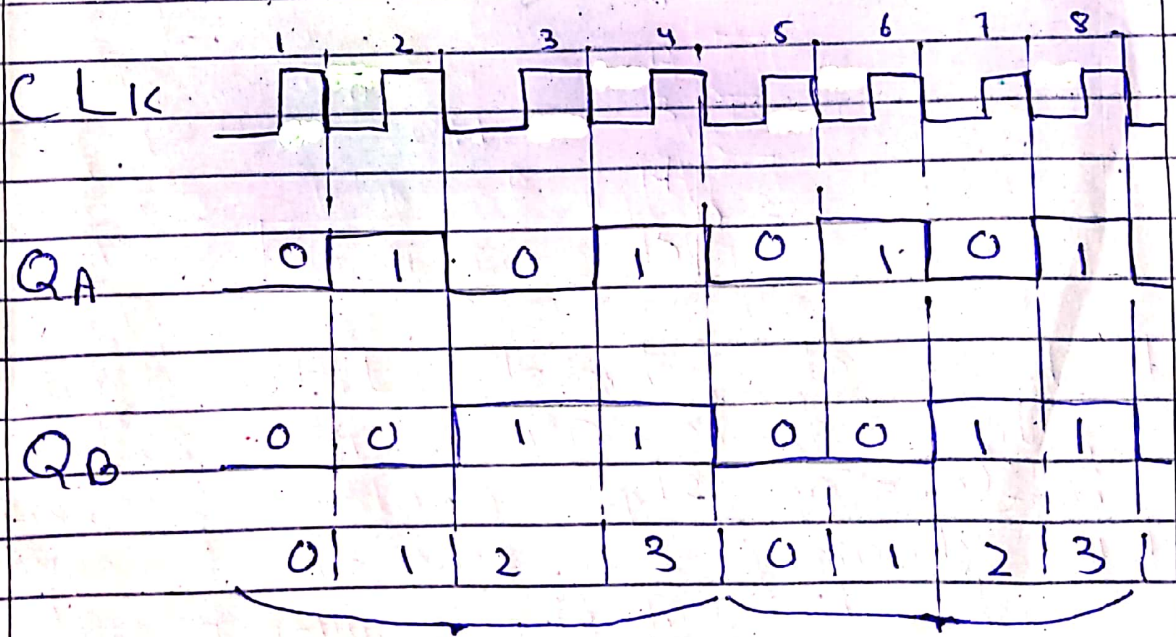
A logic symbol for a 4-line to 16-lines (1-of-16) decorder with active low output is shown in diagram. The BTN/DEC Label indicates that a binary input makes the Corre-sponding decimal output active.

Logic Diagram 4 bit active decoder

Q7. Draw and explain the logic daigram for frequency divider (use 3 J-K flip-flops and assum 16 KHZ frequency.

Ans. 7





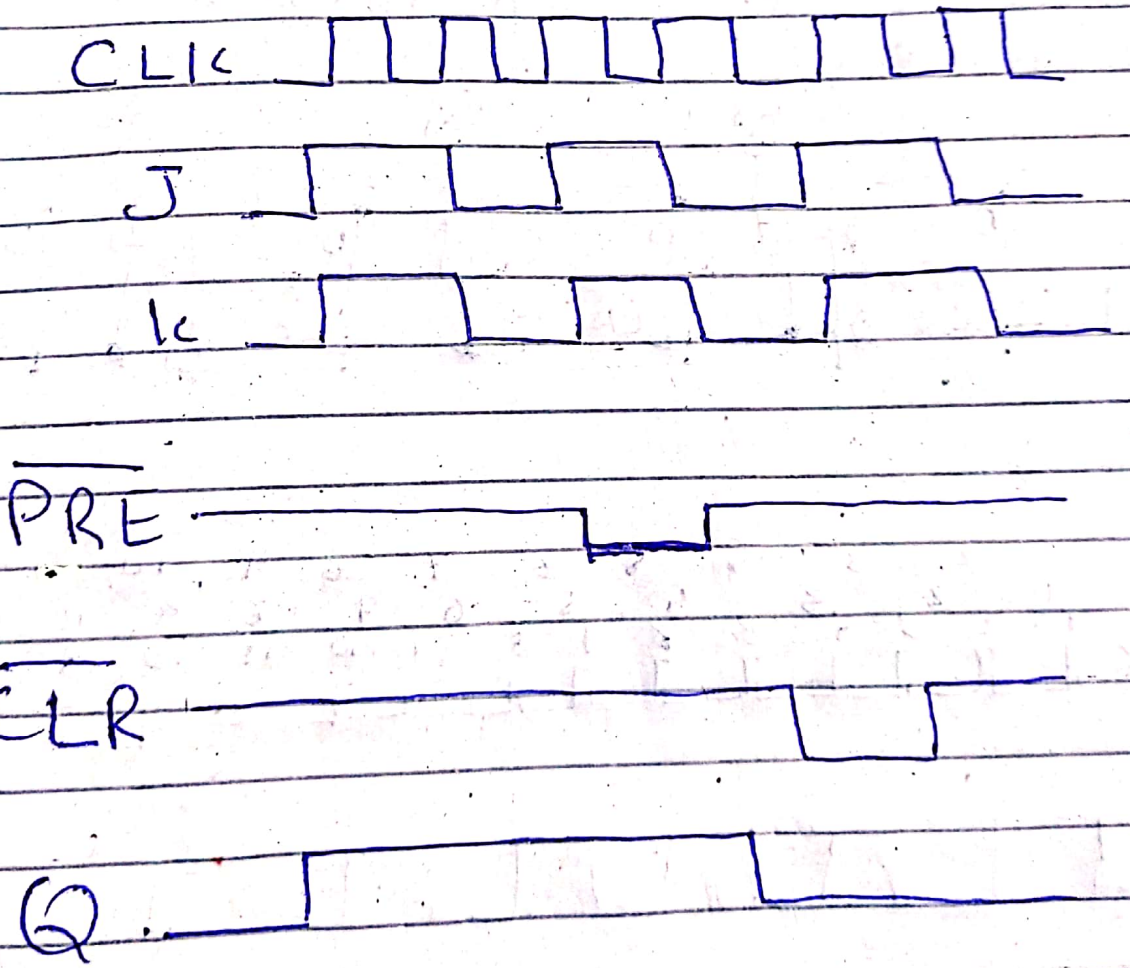
Binary sequance

Binary sequence

The logic diggram for frequency divider using 3 J-K flip floops and assume 16 KHz frequecy of the initial wave form. the negative edge triggered J-K flip floops are used for illustrate. Both flip floop are initlly RESET. flipflop A toggles on negative going transition of each clocle pulse. The Q output the flip floop A clocks flip floop B, so each time QA makes High to Low transition, flip floop B toggles. The resulting QA and QB wave forms are shown in the digram.

Q8)- Determine Q waveform relative to the clock ---- --- -Assum that is Q initially Low-

Ans) Sol)



Q9) Draw the logic daigram and timing diagram for the 4 stage Synchronous — — — — number after each clock pulse -

Ans) Four bit Synchronous Counter,