Q.(1) Give answer to the following Question :-

(A). Discuss the two to approaches for dealing with multiple interrupts

Ans:- The first is to disable interrupts while an interrupts is being processed. A disabled interrupt simply means that the processor can and will ignore that interrupt request signal.

The drawback to the preceding approach is that it does not take into account relative priority or time critical needs.

2) A second approach is to define priorities for interrupt and to allow an interrupt of higher priority

to cause a lower interrupt handler to be itself interrupted.

(13) Discuss the type of exchange that are needed by including the major process memory and I/O modules?

Ans:- The type of exchange that are needed by indicating the major forms input output processor memory and I/O modules are

Memory Processor:- The process read an instruction or a unit of data from memory processor to memory and the processor.

Processor to memory:- The processor writes a unit of data to memory.

I/O to processor:- The processor read data from an I/O device via an ~~to~~ or I/O module.

Processor to I/O:- To processor send data to the I/O device.

I/O to or from memory:- For these two an I/O module is allows to exchange data directly with memory without going through the processor using directly memory access.

(C) Discuss the QuickPath Interconnect (QPI) Protocol layers?

Ans:- QPI Protocol layers In this layer the packet is defined as the unit of transfer. One key function performed at this level is a cache coherency protocol, which deals with making sure the values held in multiple caches are consistent. A typical data packet payload is a block of data being sent to or from a cache.

D. Discuss Physical and logical Architecture PCIe in detail.

Ans:- Physical and logical Architecture PCIe

* A root complex device also referred to as a chipset or a host bridge connects the processor and memory subsystem to the PCI Express switch fabric comprising one or more PCIe and switch device.
* PCIe links from the chipset may attach to the following kind of devices that implement a PCIe.
* Switch:- The switch manages multiple PCIe

* **Pcie endpoint**:- An I/o device or controller that implement Pcie such as Gig Gigabit ethernet switch a graphics or video controller disk interface or communication controller.
* **Legacy and Point**:- legacy and point category is tended for existing designs that have been migrated to Pcl express and it allows legeay behaviors such as use of I/o space and locked transactant.
* **Pcie / Pcl brig bridge**:- Allows older Pcl devices to be connected to Pcie based system

Q(2)- Write short note on each of the following:

(A):- Instruction cycle.

Ans- The process required for a single instruction is called instruction cycle. Using the simplified Two-Step description given depided. The two steps are referred to as the fetch cycle and exute cycle Program execution hang over it the

Machine is turned off some sort of un recoverable error occurs or a program instruction that halts the computer is encountered.

(9) Instruction cycle and state diagram?

Ans:- Instruction cycle state digram.

The in instruction cycle can be described as ~~the state~~ follows

* Instruction address calculation (IAC):- Determine the address of the next instruction to be excuted usually this involves adding a fixed number to the address of the previous instruction.

* Instruction fetch (If):- Read instruction from its memory location into the processor.
* Instruction operation decoding (IOD):- Analyze instruction to determine type of operation to be performed operand processing
* Operand fetch (OF):- Perform the operation from memory. Indication

* In the instruction operand store (OS) is write the result into memory or out to input/output.

c) Classes of interrupt:-

Ans:- Classes of interrupt :-

I) Program:- It is generated by some condition that occur as a result of an instruction execution such as arithmatic overflow division by zero attempt to execute an illegal machine instruction or reference outside a user's allowed memory space.

II) Timer:- It is generated by a time within the processor. This allows the operating system to perform certain function on a regular basis.

III) I/O :- It is generated by I/O controller to signle normal completion of an operation request service from the processor or to signal variety of error condition

IV) Hardware failure :- It is generated by failure such as power or memory parity error.

(D) BUS interconnection schemes

A-5) Bus interconnection schemes

The most common computer interconnection structures are based on the use of one or more system buses.

a) **Data lines:-** The data lines provide a path for moving data among system modules. These lines collectively called the data bus.

b) **Address lines:-** The address lines are used to designate the source or destination of the data on the data bus. The width of address bus determines the maximum possible memory capacity of the system.

c) **Control lines:-** The control lines are used to control the access to and use of data and address lines. Because the data and address line are shared by all components. Typical control lines include: memory write, memory read, I/O write, I/O read, transfer ACK, Bus grant, interrupt

Q(3) :- Differentiate each of the following :-

A Program flow of controle without interupt and with interupt

Ans:) Program flow of control without interupt and with interupt

① In the Interupt cycle of Processor check to see if any interupt have accured indirected by the Pressuce of an interupt Signal.

⇒ If no interupt are pending to processor proceeds to the fitch and fetch the next instruction of the current Program.

B, Disabled interupt and nessal interrupt processing.

Ans B : Disabled interupt nessed interrupt

Dissabled interupt of simply mean that the Processor cann and will ignore that interrupt request signal

Nessed interrupt of is to allow in interrupt of higher Priority handler to be itself interrupted

C) Programing hardware and Programing software

Ans: Programing in Hardware to

Suppose we Construct a general purpose configuration of arithmatic and logic function. this set of Hardware will Perform various function of data in the original case of Customized Hardware, the system accept data and produced result

= Programing in Software.

the New Methode Programing is much easier instead of rewriting the Hardware for each code is in effort an instruction and Part of the Hardware interrupt each intruction and gener. control signal

Q(4)- Solve each of the following

(A)- The PT hypothetical machine of his two I/O intution.

0011 = load Ac from I/O

0111 = Store Ac. to I/O

in these cases the bit address indefinate a particular I/O device Show the Programme execution fusing the formal ichuction particular

I/O device. Show the program execution using the figure 3.5 for the following program

Load AC from device 5
Add content of memory 940
Store AC to device 6

Assume that the next value retved from device 5 is 3 and that location 940.

Ans:- (A) Memory (content in hex) 300: 3005; 301: 5940; 302: 7006 step 1: 3005 → IR; step 2: 3 → AC step 3: 5940 → IR; step 4: 3+2 = 5 → AC step 5: 7006 → IR; step 6: AC → device 6

(B) The program execution of figure 02 is described in the text six steps.

Ans:- Step Size :-

1) (a) The PC contains 300 the address of the first instruction This value is loaded into the MAR.

(b) The value in location 300 (which is the instruction with the value 1940 in hexadecimal) is loades into the MBR.

and the PC is interconnected. These two steps can be done in Parallel

(c) The value in the MBR is loaded into the IR.

(2) (a) The address position of the IR (9h0) is loaded into the MAR.

(b) The value in location 9h0 is loaded into the MBR.

(c) The value in the MBR is loaded into the AC.

(3) (a) The value in the PC (301) is loaded into the MAR

(b) The value in location 301 is the instruction with the value (59h1) is loaded into the MBR. and the PC is incremented.

(c) The value in the MBR is loaded into the IR.

(4) (a) The address position of the IR (9h1) is loaded into the MAR

(b) Value in location 9h1 value is loaded into the MBR.

(c) The value of location MBR are added and the result is stored

5. (a) The value in the PC (302) is loaded into the MAR.
(b) The value in location 302 (which the instruction with the 2941) is located into the MBR and the PC is incremented.
(c) The value in the MBR is located into the IR.

6. (a) The address position of the IR (2941) is located into the MAR
(b) The value in the AC is located to MBR
(c) The value in the MBR is stored in location 941.

7. How many bits are needed for the program and the instruction registers?
Ans (a) 2^{24} = 16 MBytes
(b) (1) if the location local address bus is 32 bits the whole address can be transferred at once and decoded in memory However because the data bus is only 16 bits. It will require 2 cycles to fetch a 32 bit instruction or operand.

② The 16 bit of the address placed on the address bus can't access the whole memory interface control is needed to latch and first part of the address and then the second part.

③ The program counted must be at least 24 bits. Typically a 32 - bits micro process will have a 32 - bits external address bus and a 32 bit Program counter onchip segment registed are used that many work with a smalled program counter if the instruction register is to contain the whole instruction. It will have to be 32 be long if it will be contain only the op code (called the op code register) then it will have to be 8 bits long.

④ Consider two micro processor having and 16 bit-wide external dat buses. respectively the two processor indentical otherwise and there bus cycle take just as long

⑤ Suppose all instruction and

operands are two by ten long. by what factor do the maximum data transfer rates differ?

(b) Repeat if half of the operand and instruction are one byte long.

Ans (a) During a single bus cycle the 8 bit micro processor transfer one byte. While the 16 bit micro processor has twice data transfer rate.

(b) Supose we do 100 transfer of operand and instruction of which 50 are one bytes long and 50 are two bytes long. The 8 bit micro processor takes $50+(2\times 16-50)=150$ bus cycle for the transfer. The 16 bit micro process requires $50+50=100$ bus cycle. Thus the data transfer rates differ by a factor of 1.5.

(c) The intel 8086 is a 16 bit processor similar in many ways to the 8 bit 8088. The 8086 used a 16 bit bus that can

transfer 2 bytes at a time provided that them could address bytes has an even address. However the 8086 allows both even and odd-aligned word operands. If an aligned word is stored two memory cycles. each consisting of four bus cycle are required to transfer the word. Consider an instruction on the 8086 that involves two 16 bits operands how long does it take to fetch the operand Give the range of the possible answers Assume a clocking rate of 4MHz and note wait states.

Ans:- A bus cycles takes 0.25 μs. So a memory cycles take 1μs. if both operand are even aligned it takes 2μs to fetch the two operand if one is odd-aligned the time required is 3μs - if both are odd aligned the time required is 4 μs.

(E) Consider a 32-bit micro processor whose bus cycle is the same duration as that of a 16-bit

micro-processor. Assume that on average 20% of the operands and instruction are 32 bits long 40% are 16 bit and 40% are only 8 bit long calculate the improvement achieved when fetching instruction and operand with the 32-bit micro-processor.

Ans:- Consider a mix of 100 instruction and operands on average they consist of 20% 32 bit items - 40% 16 bits items and 40% 8 bit item The number of bus cycle required for the 16 bit micro processor is (2×20)+40+40 = 120. For the 32 bit micro processor the number required is 100. This amount to an improvement 20/120 or about 17%.