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Subject Digital logic design

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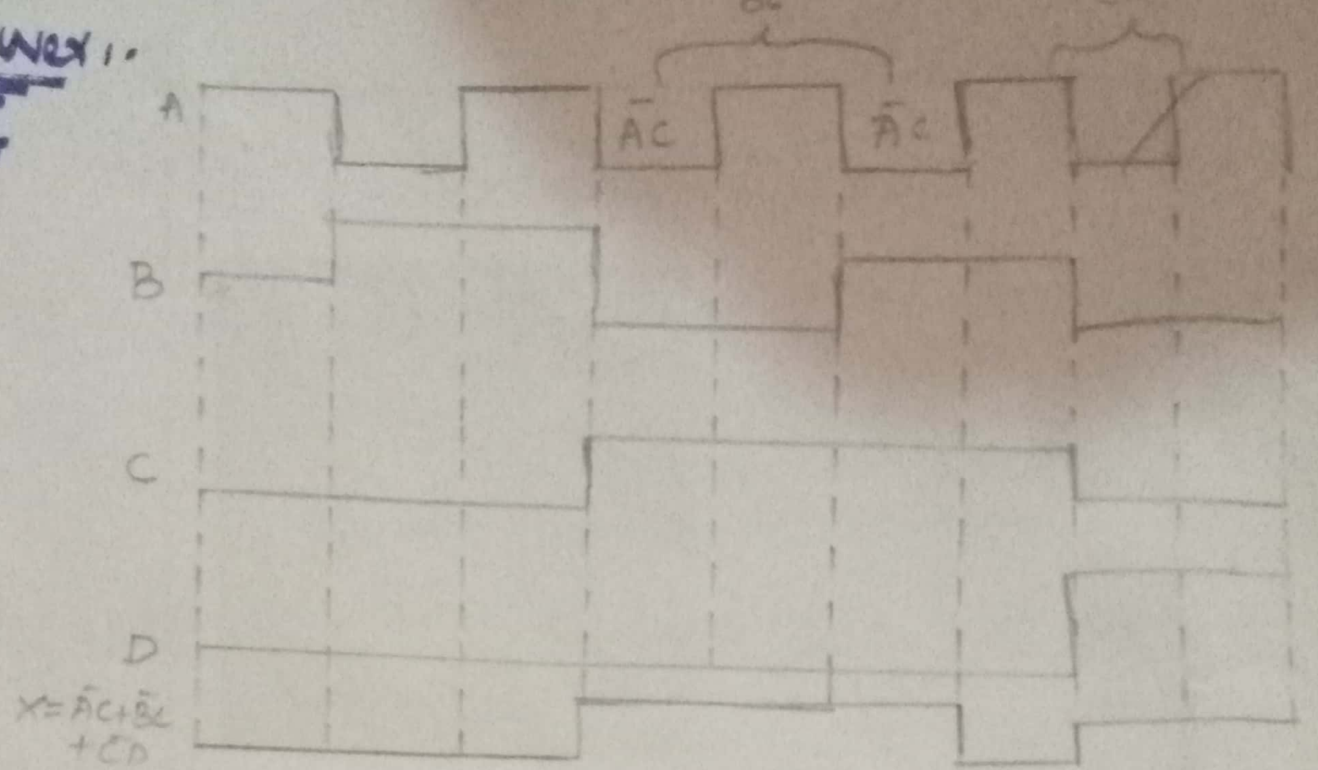
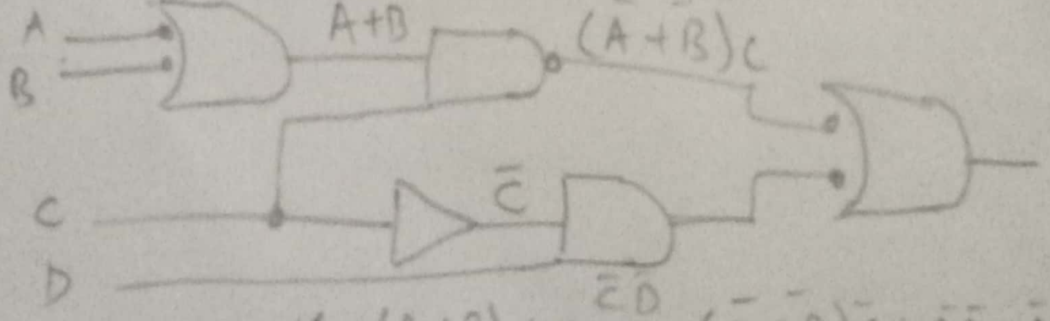
Q1 Draw the logic circuit ... — ... — — ... - - - waveform Figure 01.

Answer:



Solution: The output expression for the circuit is developed in The SOP form indicates that the output is high when A is low a C is HIGH or when B is low and C is High or when C is Low and D is HIGH.



$X = \overline{(A+B)}C + \bar{C}D = (\bar{A}+\bar{B})C + \bar{C}D = \bar{A}C + \bar{B}C$

Q→02 For the 4-input multiplexer data input are given.

Ans:-

A 4x1 Multiplexer has 4 input lines (D_0, D_1, D_2, D_3) two select input (S_0 and S_1) and one output line y.

If $S_1S_0 = 00$ then $Y = D_0$

If $S_1S_0 = 01$ then $Y = D_1$

If $S_1S_0 = 10$ then $Y = D_2$

If $S_1S_0 = 11$ then $Y = D_3$

Data Input		output.
S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

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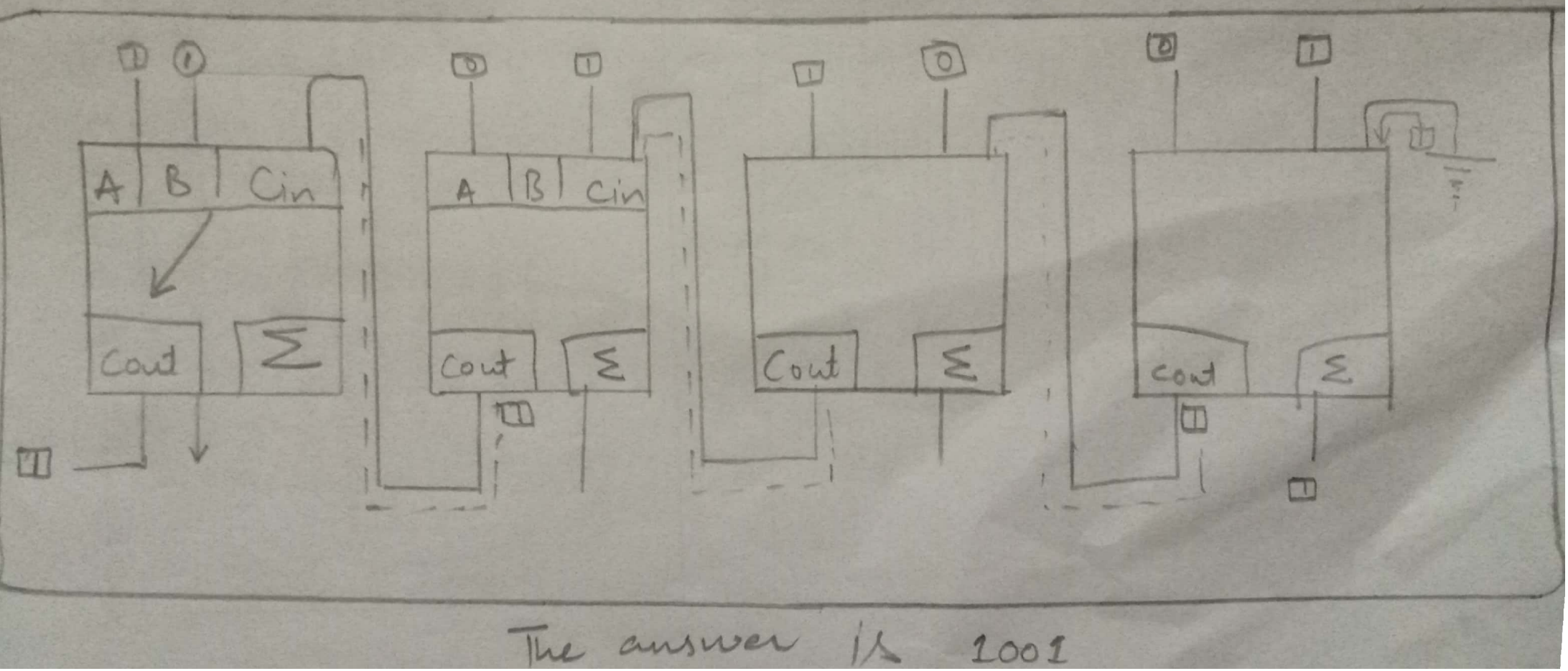
Question No → 03



The answer is 1001

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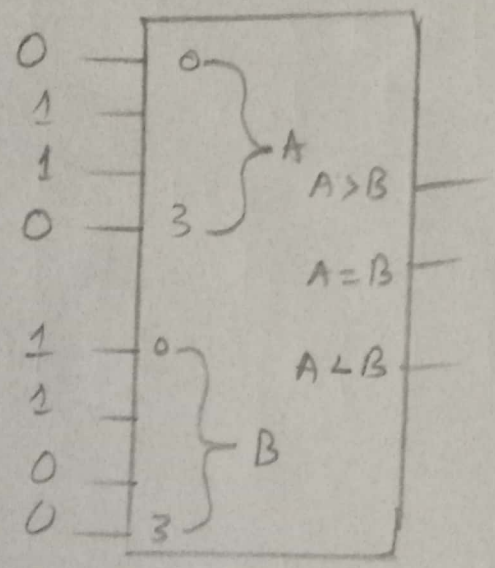
Question No ⇒ 04 :- Determine A=B, A>B and A<B output for the input number show on the comparator in Figure 03:.

Ans- Determine the A = B, A > B, A < B outputs for the input numbers show on comparator in Figure.



Solution: The number on the A inputs is 0110 and the number on the B inputs is 0011. The ~~input~~ output is HIGH and the other outputs are low

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Question No ⇒ 05:- Show the logic required to ..... code word to binary 1011:-

Solution:-

① The MSB is kept the same

② Next take the XOR of the first and the second binary bit

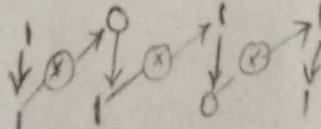
③ Next take the XOR of the second and third binary bit.

④ Next take the XOR of

⑤ Lastly take the XOR of the fourth and fifth binary bit.

Gray code of binary conversion:-

$g(3)\ g(2)\ g(1)\ g(0)$



(Gray)

(Binary)

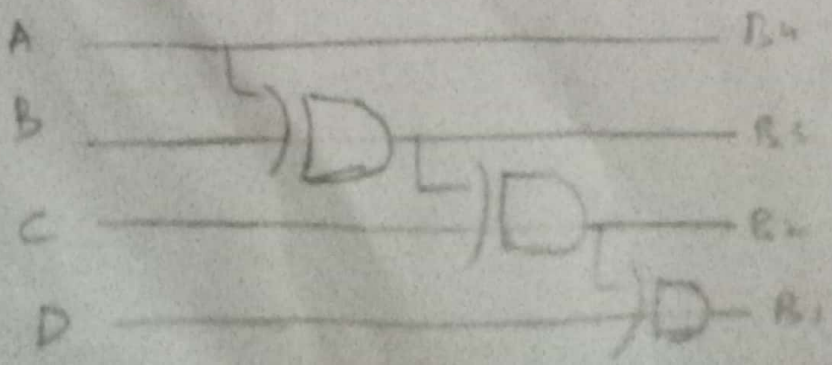
$B(B)\ (B_2)\ (B_1)\ (B_0)$

$b(3) = g(3)$

$b(2) = b(3) \oplus g(3)$

$b(1) = b(2) + g(1)$

$b(0) = b(1) + g(0)$



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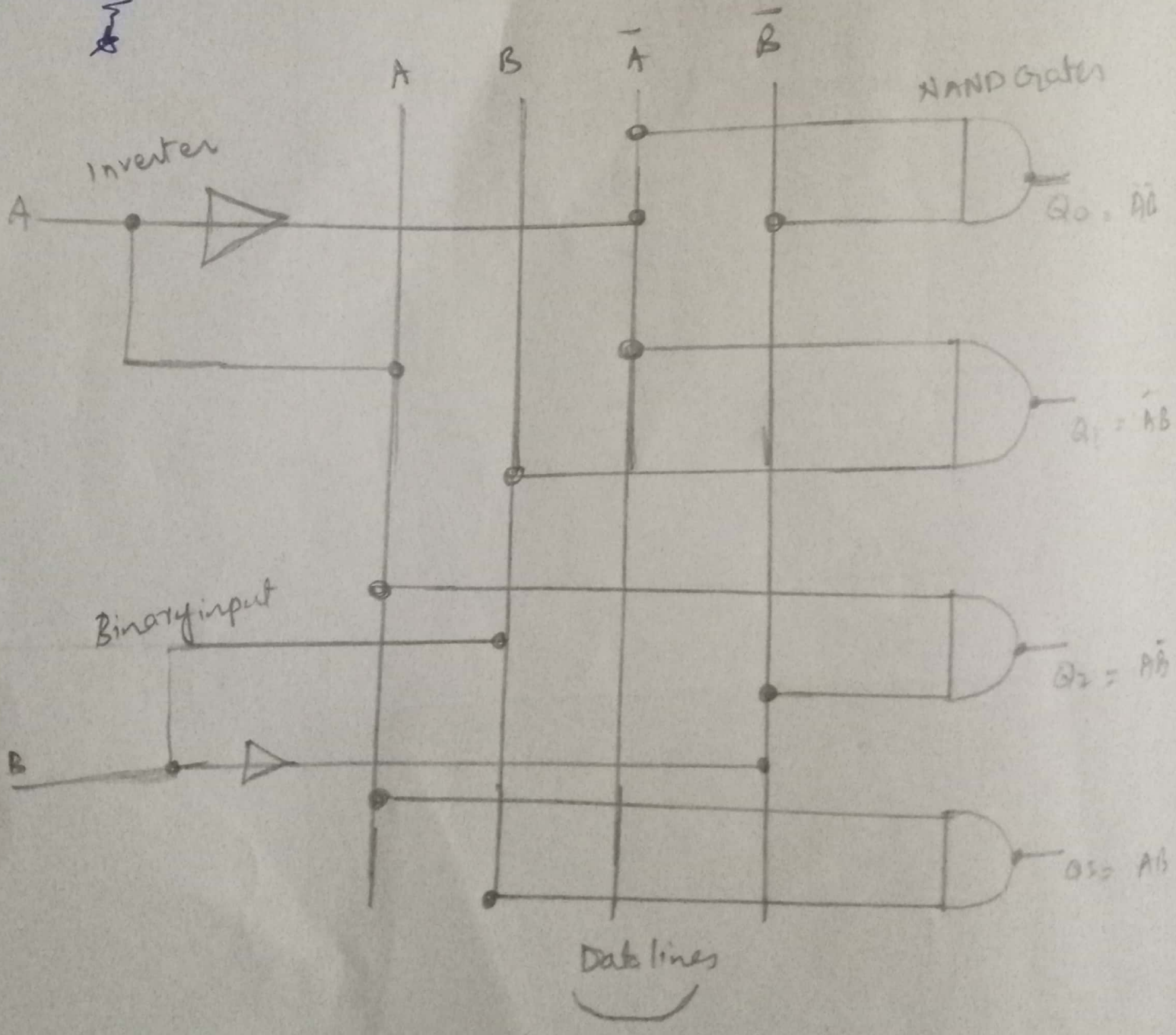
Question No ⇒ 06:- Draw and explain logic diagram for 4 bit active low decoder?

Solve:-



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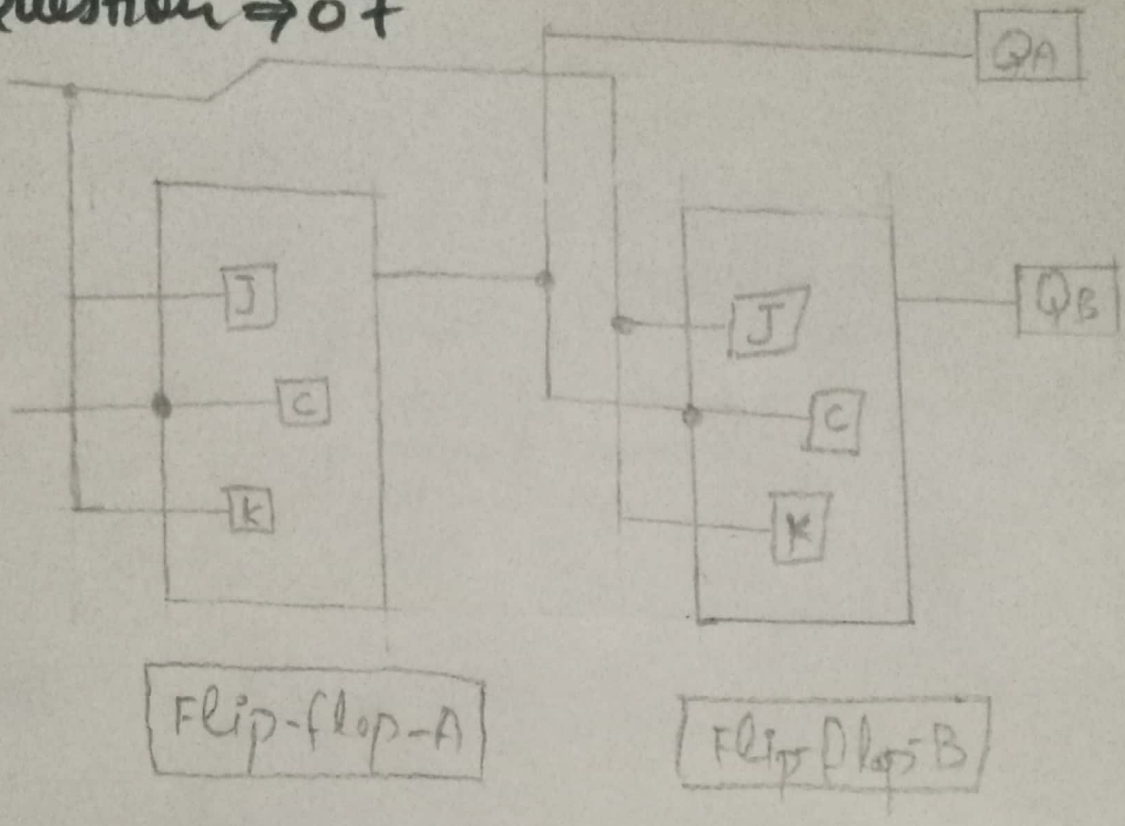
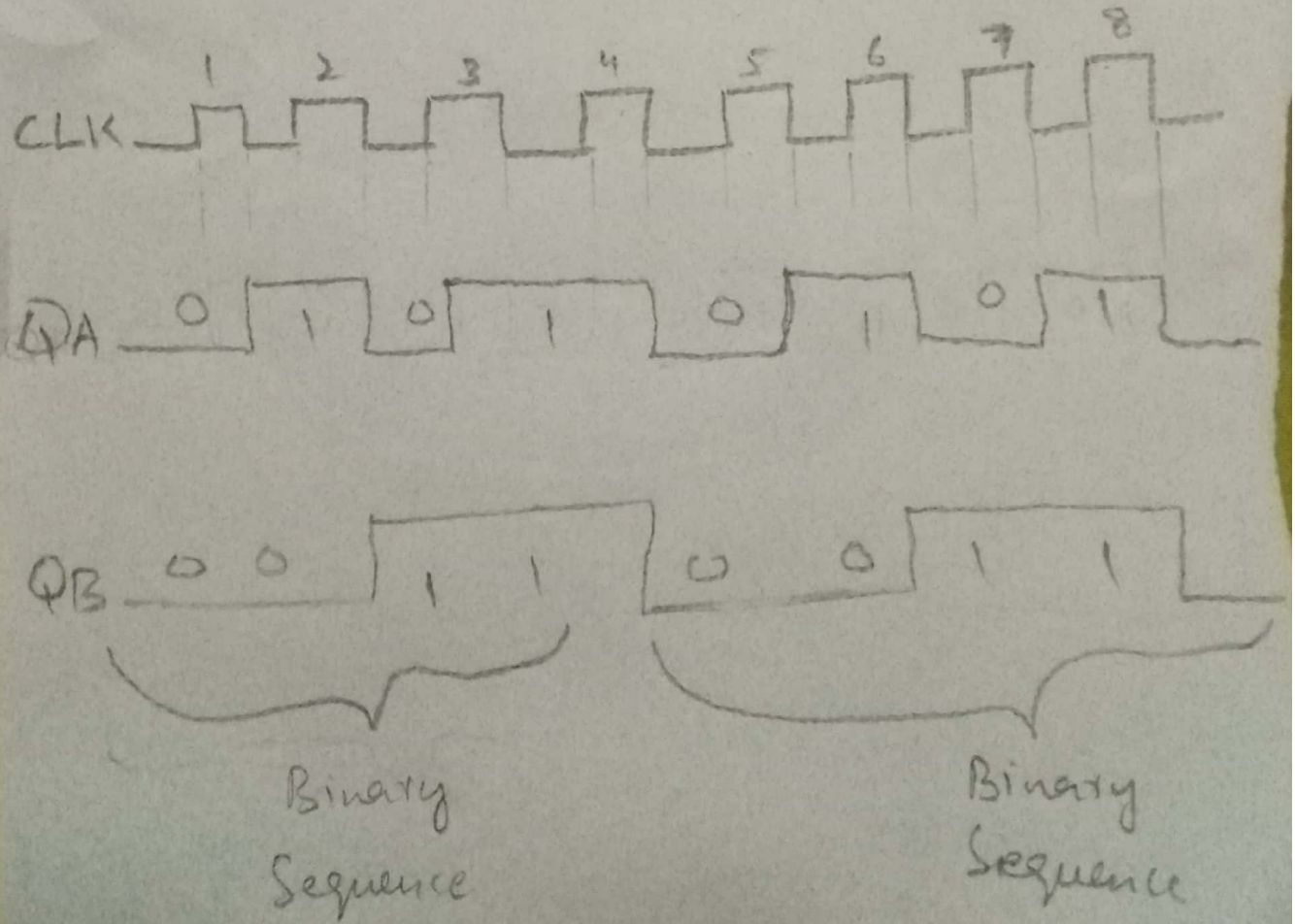
Question ⇒ 07





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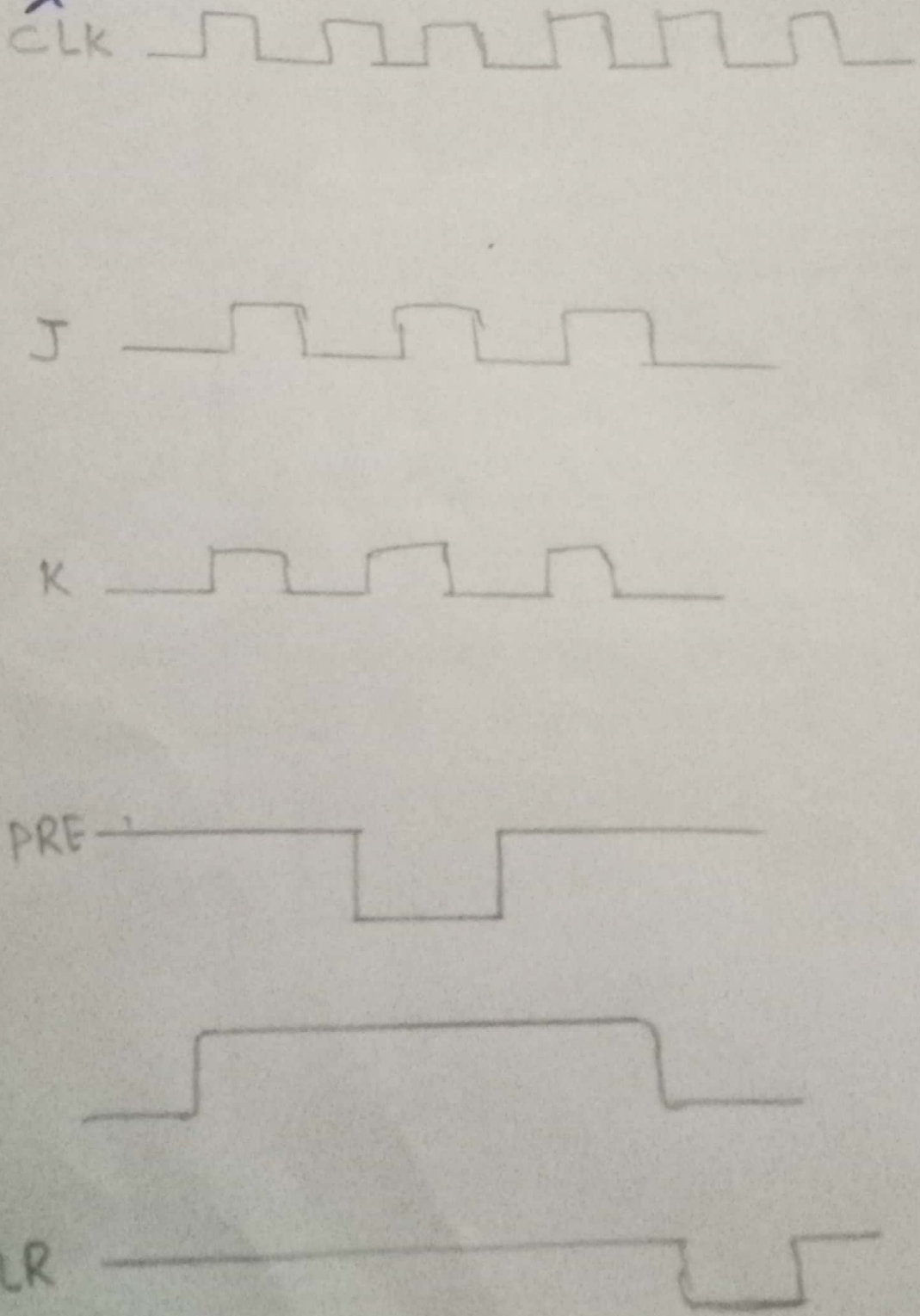
Question No # 08:- Determine the Q waveform relative to the clock of the style ~~~ ~~~ Q is initially low.

Solve



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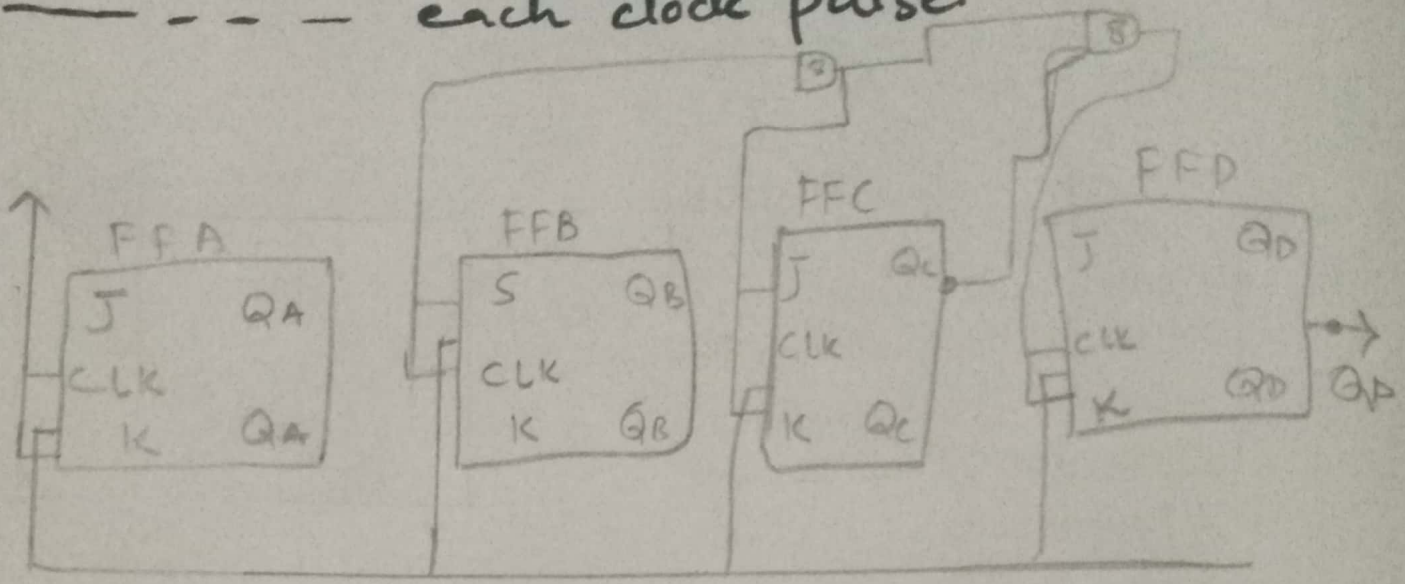
Question No ⇒ 09 Draw the logic diagram and timing diagram for 4-stage synchronous ——— - - - each clock pulse.



It can bee seen above that the external clock pulse are feed directly to each of the J-K flipflops in the clock chain both the J and K inputs J-K inputs of flip-flop (FFB) are connected to output QA of (FFA) but J-K input of (FFC) and (FFD) are driven from Seprate AND gates which also supplies with signals from input and output of the previces stage.

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