Day: M T W T F S Date: __/__/__

NAME JIBRAN
ID 14472
SUBJECT COMPUTER ARCHITECTURE
DEPARTMENT BS(CS)
SEMESTER 4th

Q (1) part (a)

(A) Here some of techniques used to increase the speed are

(1) Pipelining:- pipelining enable to processor to work simultaneously on multiple instruction by performing a different phase for each of the multiple instruction.

(2) Branch prediction:- Branch prediction potentially increase the amount of work available for the processor to execute.

(3) Superscaler execution:- This is the ability to issue more than one instruction in every processor clock cycle.

(4) Data flow analysis:- The processor analysis which instruction are dependent on each other results or data to create an optimized schedule of instruction.

Day: M T W T F S Date: __/__/__

(5) Speculative execution. This enables the processor to keep its execution engines as busy as possible by executing instruction that are likely to be needed.

Q (1) part (b).

Amdahl's law:-

is often used in parallel computing to predict the theoretical speedup when using multiple processors. For example, if a program needs 20 hours to complete using a single thread, but a one hour portion of the program cannot be parallized, therefore only the remaining 19 hours ($p = 0.95$) of execution time can be parallized, then regardless of how many threads are devoted to a parallized execution of this program, the minimum execution time cannot be less than one hour. Hence, the theoritical speedup is limited to at most 20 times the single thread performance.

Day: M T W T F S Date: __/__/__

Q(1) part (c).

QPI protocol layers:-

In this layer, the packet is defined as the unit of transfer. One key function perform at this level in a cache coherency protocol, which deals with making sure that main memory values held in multiple caches are consistant. A typical data packet payload is a block of data being sent to or from a cache.

Q(1) part (d)

Physical and logical Architecture of PCIe.

* A root complex device also refered to as a chipset or a host bridge connect the processor and many subsystem to the PCI Express switch fabrics comparising one or more PCIe and PCIe switch device.
* PCIe links from the chipset may attach to the following kind of devices that

Day: M T W T F S Date: __/__/__

implement PCIe.

* Switch: The switch manages multiple PCIe streams.
* PCIe endpoints: An I/O devices or controller that implement PCIe such as eligibit ethernet switch a graphics or video constructor dock interface or a communication controller.
* PCIe/PCI bridge: Allow order PCI devices to be connected to PCIe-based systems.

Q(2) part (a)

Consequences of Moore's law.

(1) The cost of a chip has remained virtually unchanged during this period of rapid growth in density. This means that the cost of computer logic and memory circuitry has fallen at a dramatic rate.

(2) Because logic and memory elements are placed closer together on more densely packed chips, the electrical path length is shortened increasing operating speed.

Day: M T W T F S

Date: __/__/__

(3) The computer becomes smaller, making it more convenient to place in a variety of environments.

(4) There is a reduction in power and cooling requirements.

(5) The interconnections on the integrated circuit are much more reliable than solder connections. With more circuitry on each chip, there are fewer interchip connections.

Day: M T W T F S Date: __/__/__

(1)

Q(2) part (b)

Key characteristics of planned computer family.

Similar or Identical instruction set:

In many cases, the same set of machine instructions is supported on all members of the family. Thus, a program that executes on one machine will also execute on any other.

* Similar or identical operating System:

The same basic operating system is available for all family members.

* Increasing speed:

The rate of instruction execution increases in going from lower to higher family members.

* Increasing Numbers of I/O ports: In going from lower to higher family members.

* Increasing memory size: In going from lower to higher family members.

Day: M T W T F S

Date: __/__/__

Q(2) part(c)

Instruction cycle state diagram:

The state in instruction cycle can be described as follows-

* Instruction address calculation (IAC) Determine the address of the next instruction to be executed. Usually this involves adding a fixed number to the address of the previous instruction.
* Instruction fetch (IF):- Read instruction from its memory location into the processor.
* Instruction operating decoding: (IOD). Analyze instruction to determine type of operation to be performed.
* Operand fetch: (OF). Fetch the operand from memory or read it in from I/O.
* Data operation (DO): perform the operation indicated in the instruction.
* Operand store (OS): Write the result into memory or out to I/O.

Day: M T W T F S

Date: __/__/__

Q(2) part (d)

Classes of interrupt:

it is generated by some condition that occur as a result of an instruction execution such as arithmatic overflow.

* Timer.

its generated by a timer within a processor this allows the operating system to perform certain function on a regular basis.

* I/O:

its generated by an I/O controller to signal normal completion of an operation request service from the processor, or to signal a variety of error condition.

Day: M T W T F S Date: __/__/__

Q (3) par (a)

Cortex - A:

The cortex - A and cortex - A50 are application processor intended for mobile device such as smartphones and ebook readers, as well as consumer device such as digital tv and home gateways (e.g DSL and cable internet modems) These processors run at higher clock frequency (over 1 GHz) and support an memory management unit (MMU).

Cortex - R:

The cortex - R is designed to support real time application in which the timing of events need to be controlled will rapid response to events. They can run at a fairly high clock frequency. (e.g 200 MHz to 800 MHz) and have very low response latency.

Cortex - M:

Series processors have been developed primary for

Checked By:..... Parents..... Excellent ☐ Good ☐ BABAR PAPER PRODUCTS

Day: M T W T F S

Date: __/__/__

the micro controller domain where the need for fast, highly deterministic interrupt management is coupled with the desire for extremely low count and lowest possible power consumption.

Q(3) (b)

(a) Multicore:

The use of multiple processors on the same chip provides the potential to increase performance without increasing the clock rate.

* ~~Strategy~~ strategy is to use two simpler processors on the chip rather than one more complex processor.
* With two processors larger caches are justified.
* As caches became larger it made performance sense to create two and then three levels of of cache on a chip.

MIC:

Leap in performance as well as the challenges in developing software to exploit such a large number of cores.

* The multicore and MIC strategy involves a homogeneous collection of general purpose processor on a single chip.

Day: M T W T F S

(12)

Date: __/__/__

GPU..

Core designed to perform parallel operations on graphics data.

* Traditionally found on a plug-in graphics card, it is used to encode and render 2D and 3D graphics as well as process video.
* Used as vector processor for a variety of applications that require repetitive computations.

(13)

Day: M T W T F S

Date: __/__/__

(Q3) part (c).

A disabled interupt simply means that the processor can and will ignore that interupt request signal.

* A nested interupts is to allow an interupts of higher priority to cause a lower-priority interrupt handler to be lower priority interupt handler to be itself interupted.

Day: M T W T F S Date: __/__/__

Q(4) part (a)

EC12 core layout:

* ISU (instruction Sequence unit).
Determine the sequence in which instruction are executed in what is referred to as a superscalar architecture.

* IFU (instruction fetch unit).
logic for fetching instruction

* IDU (instruction Decode unit).
The IDU is fed from the IFU buffers and is responsible for the parsing and decoding of all architecture operation code.

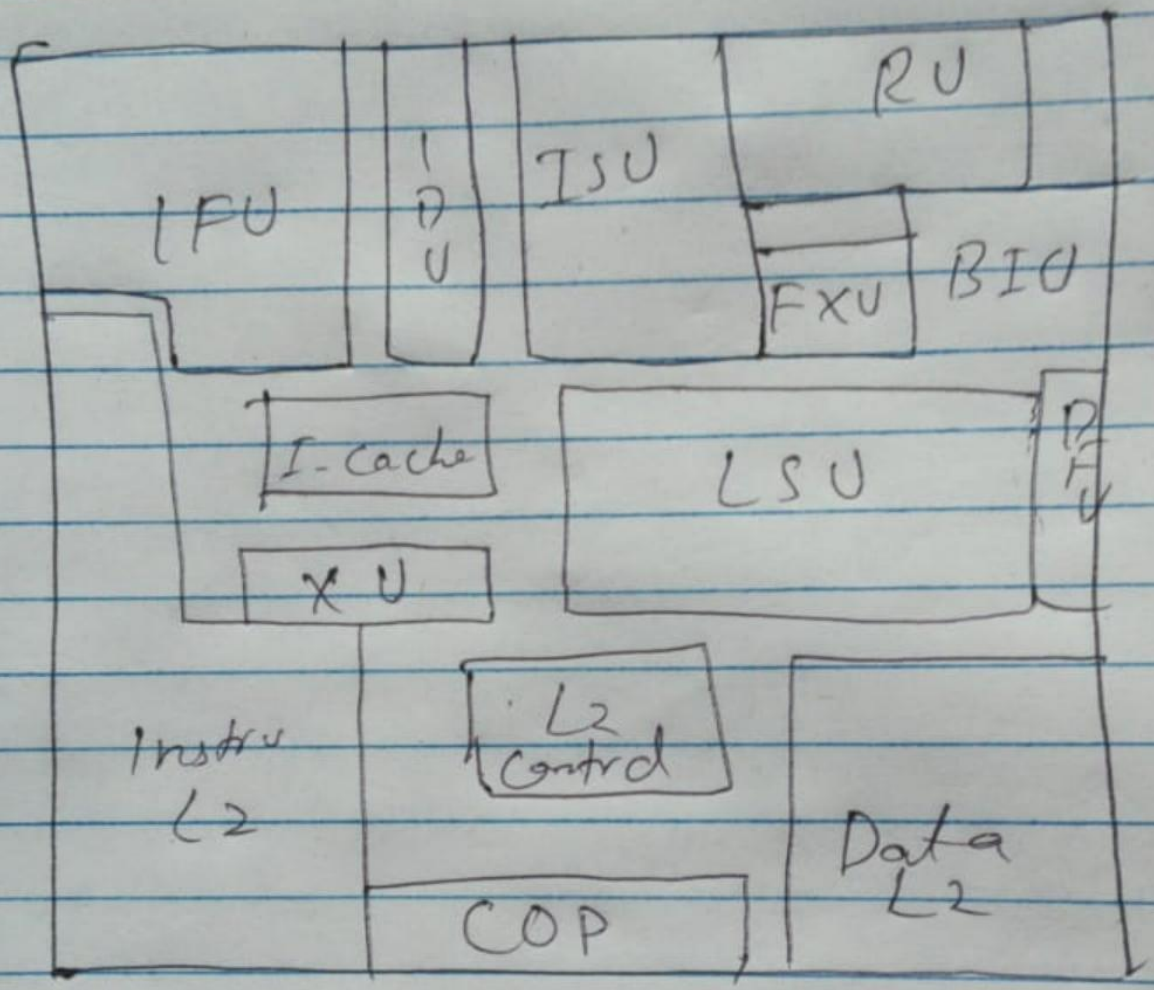
* LSU (load store unit):
its responsible for handling all types of operand access of all length, modes, and formats as defined in all z/architecture.

* FXU (Fixed point unit):-
The FXU execute fixed point arithmatic operations.

16

Date: __/__/__

TWTFS



(44)

(15)

Day: M T W T F S

Date: __/__/__

Q(4) part (b)

Discuss the IAS operation in detail.

The IAS operates by respectively performing an instruction cycle. Each instruction cycle consist of two sub-cycle.

* Fetch Cycle:-
The opcode of the next instruction is loaded into the IR and the address portion is load into the MAR. This instruction may be taken from the IBR, or it can be obtained from memory by loading a word into the IBR, IR & MAR.

* Execute Cycle:-
The control circuitry interprets the opcode and executes the instruction by sending out the approximate control signals to cause data to be moved on a operation to be performed by the ALU.

Day: M T W T F S

Date: __/__/__

Q(5)

Solution:-

Effective CPI:

$$CPI = \frac{(1 \times 46000) + (2 \times 33000) + (2 \times 16000) + (2 \times 9000)}{100}$$

$$CPI = \frac{162000}{100}$$

$$CPI = 1620$$

MIPS Rate:

$$\text{MIPS rate} = \frac{60\ MHz}{1620 \times 106}$$

$$\text{MIPS rate} = \frac{60 \times 106}{1620 \times 106}$$

$$\text{MIPS rate} = \frac{60}{1620}$$

$$\text{MIPS rate} = 0.037$$

Execution time:

$$T = \frac{Ic}{(MIPS \times 106)}$$

$$T = \frac{104000}{0.037 \times 106} = \frac{104000}{37 \times 103}$$

$$T = 2811 \times 10^{-3} = \boxed{2.811\ sec}$$