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ID: 14726

Subject: Computer Architecture

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Q1a) Word:-

The "natural" unit of organization of memory. The size of word is typically equal to the number of bits used to represent an integer and to the instruction length

- Addressable units:-

In some system, the addressable unit is the word. However, many systems allow addressing at the byte level. In any case, $2^A = N$.

- Unit of transfer:-

For main memory, this is the number of bits read out of or written into memory at a time. The unit of transfer need not equal a word or an addressable unit.

M. Bilal

I.D 14726 P(2)

Q1 a)

the SRAM address line is used to open or close a switch. The address line ~~controller~~ controls two transistors (T5 and T6). When a signal is applied to this line, the two transistors are switched on, allowing a read or write operation.

For a write operation, the desired bit value is applied to line B, while its complement

Q1 b) Reasons for DVD's greater capacity over CD

The DVD's greater capacity is due to three differences from CDs:

1. Bits are packed more closely on a DVD. The spacing

M. Bilal

I.D 14726 P(3)

between loops of a spiral on a CD is 1.6 μm and the minimum distance between pits along the spiral is 0.834 μm. The DVD uses a laser with shorter wavelength and achieves a loop spacing of 0.74 μm and minimum distance between pits of 0.4 μm. The result of these two improvements is about a seven-fold increase in capacity, to about 4.7 GB.

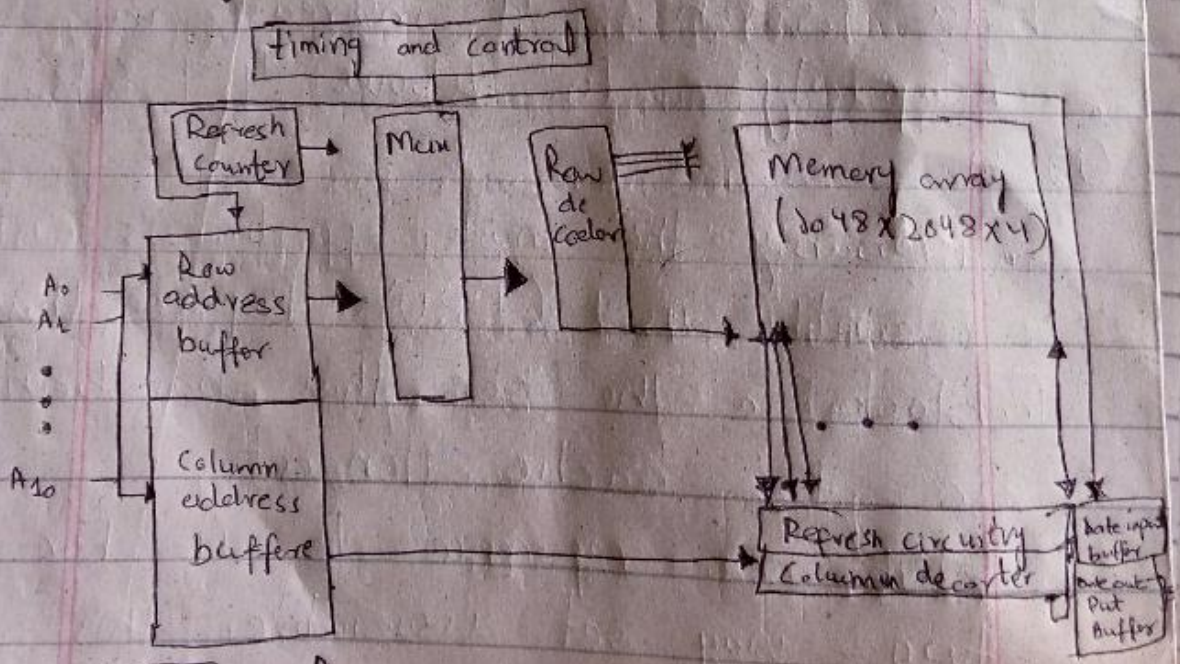
Q2 b)

. Probably the most effective is least recently used (LRU): Replace that block in the set that has been in the cache longest with no reference to it. For two-way set associative, this is easily implemented.

Each

line includes a USE bit. When a line referenced, its USE bit is set to 1 and the USE bit of the other line in that is set ~~is~~ to 0. When a block to be read into the set, the line whose USE bit is 0 is used.

Q2(d) Discus 16-Mbit DRAM(4M×4) organization using diagram



Typical 16-Mbit DRAM (4M×4)

M. Bilal

I.D 14726 P(5)

Chip while all data cells are refreshed. The refresh counter, steps through all of the row values. This causes each cell in row to be refreshed.

M.Bilal

ID 14726

P(6)

Q2

a) Hard failure

A hard failure is a permanent physical defect so that the memory cell or cells affected cannot reliably store data but become stuck at 0 or 1 or switch erratically between 0 and 1. Hard errors can be caused by harsh environmental abuse, manufacturing defects, and wear.

b) Soft error:

A Soft error is a random, nondestructive event that alters the contents of one or more memory cells without damaging the memory. Soft errors can be caused by power supply problems or alpha particles. These particles from

distressingly Common because radioactive nuclei are found in small quantities in nearly all materials.

Both hard and soft errors are clearly undesirable, and most modern main memory systems include for both detecting and correcting errors.

Q2< Magnetic disk read and write Mechanisms.

Read

The traditional read mechanism exploits the fact that a magnetic field moving relative to a coil produces an electrical current in the coil. When the surface

of the

disk passes under the head, it generates a current of the same polarity as the one already recorded.

Q2 d) Parallel access and independent access RAID schemes.

Parallel access: All member disks participate in the execution of every I/O request. Typically, the spindles of the individual drives are synchronized so that each disk head is in the same position on each disk at any given time.

Independent access: Each member disk operates independently, so that separate I/O requests can be satisfied in parallel.

M. Bilal

I.D 14726 P(9)

Q2(e) HD DVD and Blu-ray DVD.

HD DVD players have been much cheaper than Blu-ray machines, but blu-ray discs have more storage space and more advanced protections against piracy.

Both versions deliver sharp resolution.

Blu-Ray has 25 GB capacity (50 GB for dual-layer) and is more expensive.

HD-DVD has 15 GB (30 GB for dual layer) and is cheaper than Blu-Ray.

ID 14726 P (10)

Q3

A. Memory Access Methods

These are 4 types of memory access methods:

1. Sequential Access:-

In this method, the memory is accessed in a specific linear sequential manner like accessing in a single Linked List. The access time depends on the location of the data.

Applications of this sequential memory access the magnetic tapes, magnetic disk and optical memories.

2. Random Access:

In this method, any location of the memory can be accessed randomly like accessing in Array. Physical locations are independent in this access method.

Applications of this random memory access are RAM and ROM.

3. Direct Access:
In this method, the particular location of the memory can be accessed directly like accessing in Array. This method is a combination of above two access methods. The access time depends on both the memory organization and characteristics of storage technology. The access is semi-random or direct.
Applications of thus direct memory access is magnetic hard disk, read/write header.

4. Associate Access:-
In this method, a word is accessed rather than its address. This accessed method is a special type of random access method. Application of thus direct

is never

memory access is Cache memory.

Q3. B.

Principle of locality

The principle of locality ~~is~~ states that data in the vicinity of a referenced word are likely to be referenced in the near future.

OR

An implication of locality is that we can predict with reasonable accuracy what instructions and data a program will use in the near future based on its accesses in the recent past.

Q3 C.

Possible approaches to cache coherency

Possible approaches to cache coherency include the following:

- Bus watching with write through: Each cache controller monitors

the address lines to detect write operations to memory by other bus masters. If another master writes to a location in shared memory that also resides in the cache.

memory, the cache controller invalidates that cache entry. This strategy depends

on the use of a write-through policy by all cache controllers.

- Hardware transparency: Additional hardware is used to ensure that all updates

to main memory via cache are reflected in all caches.

Thus, if one processor

modifies a word in its cache, this update is written to main memory. In addition,

any matching words in other caches are similarly updated.

- Non-cacheable memory:-
  Only a portion of main memory is shared by more

than one processor, and this is designated as non-cacheable. In such a system,

all accesses to shared memory are cache misses, because that shared memory

M. Bilal

I.D 14726 P(15)

The non - cacheable memory can be identified

Using chip - select logic or high - address bits.

Q3 D.

There are two practical issues peculiar to SSDs that are not faced by HDDs:

- SSD performance has a tendency to slow down as the device is used
- The entire block must be read from the flash memory and placed in a RAM buffer.
- Before the block can be written back to flash memory, the entire block of flash memory must be erased.
- The entire block from the buffer

memory.

- Flash memory becomes unusable after a certain number of writes
- Techniques for prolonging life:
- Front-ending the flash with a cache to delay and group write operations.
- Using wear-leveling algorithms that evenly ~~distribute~~ distribute writes across block of cells.
- Bad-block management techniques
- Most flash devices estimate their own remaining lifetimes so systems can anticipate failure and take preemptive action

Q3E.

Discuss the CD read and write operation.

Read

Information is retrieved from a CD or CD-ROM by a low-powered laser housed in an

optical- disk player, or drive unit. The laser shines through the clear Polycarbonate while a motor spins the disk past it. The intensity of the reflected light of the laser changes as it encounters a pit.

beam falls on a pit, while has a somewhat rough surface, the light scatters and low

A land is a smooth surface, while reflects back at higher intensity. The change

between pits and lands is detected by a photo sensor and converted into a digital

Signal. The sensor tests the

I.D 14726 P(18)

the surface at regular intervals. The beginning or end of

a pit represents a 1; when no change in elevation occurs between intervals, a 0 is recorded.

Write
Recall that on a magnetic disk, information is recorded in concentric tracks.

With the simplest constant angular velocity (CAV) system, the number of bits per

track is constant. An increase in density is achieved with multiple zoned recording.

Increases capacity, it is still not optimal.

I.D 14726 P(19)

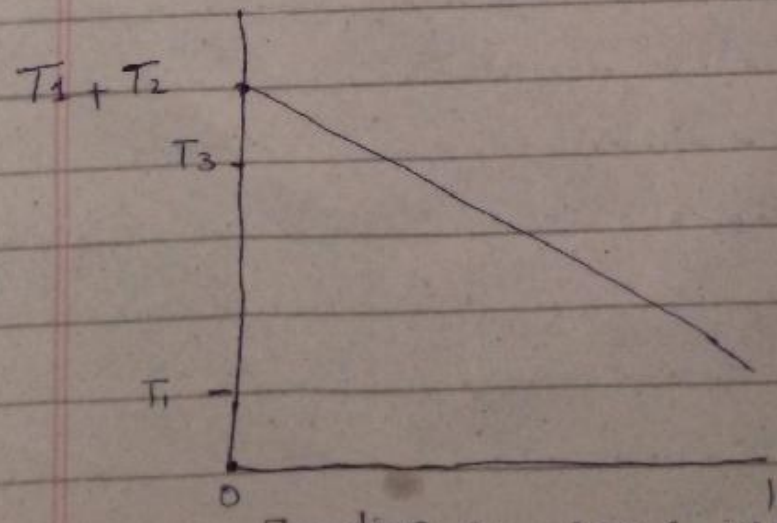
Q4a)

In our example, Suppose 95% of the memory accessor are found in level 1. Then the average time to access a word can be expressed as

$(0.95)(0.01\,\mu s) + (0.05)(0.01\,\mu s + 0.1\,\mu s) =$

$0.0005 + 0.0055 = 0.015\,\mu s$

The average access time is much closer to 0.01 μs then to 0.01 μs as desired



Fraction of acess involving only level 1 (bit ratio)

M Bilal

I.D 14726

Q4 b) Tag (9) /set (B) /word (2)

Total block in the cache =

8kbytes /16bytes = $2^3 \times 2^{10} / 2^4 =$

$2^9 = 512$

Number of set = number of block in cache / 2

Number of set = 512/2

Number of set = 256

Number of set = 2^8

Number of set = 8

Size of block = 16 = 2^4

Size of memory = $2^6 \times 2^{20} = 2^{26}$

Tag = size of memory − set − size of block

Tag = 26 − 8 − 4

Tag = 14

tag	set	size of block
14	8	4

Q4d

M = 8

$2^k - 1 >= k + m$

$2^4 - 1 >= 4 + 8$

$15 >= 12$

M. Bilal

I.D 24726

1	2	3	4	5	6	7	8	9	10	11	12
1	0	1	1	1	0	0	1	0	0	1	0

The check bits are in a bit numbers: 1, 2, 3, 4 and 8

- Check bit 8 calculated by values in bit numbers: 9, 10, 11 and 12
- Check bit 4 calculated by values in bit numbers: 5, 6, 7 and 12
- Check bit 2 calculated by values in bit numbers: 3, 6, 7, 10 and 11
- Check bit 1 calculated by values in Bit numbers: 3, 5, 7, 9, 10 and 11. Thus, the check bit are: 1011

Q4 d.

Sol

7200 revolution in 60 sec

1 revolution in $\frac{60}{7200}$ OR

1 revolution in 6ms

M. Bilal
I.D 14726

P(21)

1 revolution = covering one entire track
500 sector

500 sector = 6ms
1 sector = 8 microsecond

Now there are 2 different things
① 2500 sectors so time = 2500 × 8ms = 20ms

② 1.28 MB = 134177.28 Bytes OR 2621.44 sectors
2622 sectors = 20.976 ms.

Total time case
case ① 4 + 2 + 20 = 26ms
case ② 4 + 2 + 20.976 = 26.976ms

M. Bilal
I D 14726

P(21)

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case (1) 4 + 2 + 20 = 26ms

case (2) 4 + 2 + 20.976 = 26.976ms