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13119

DLD LAB

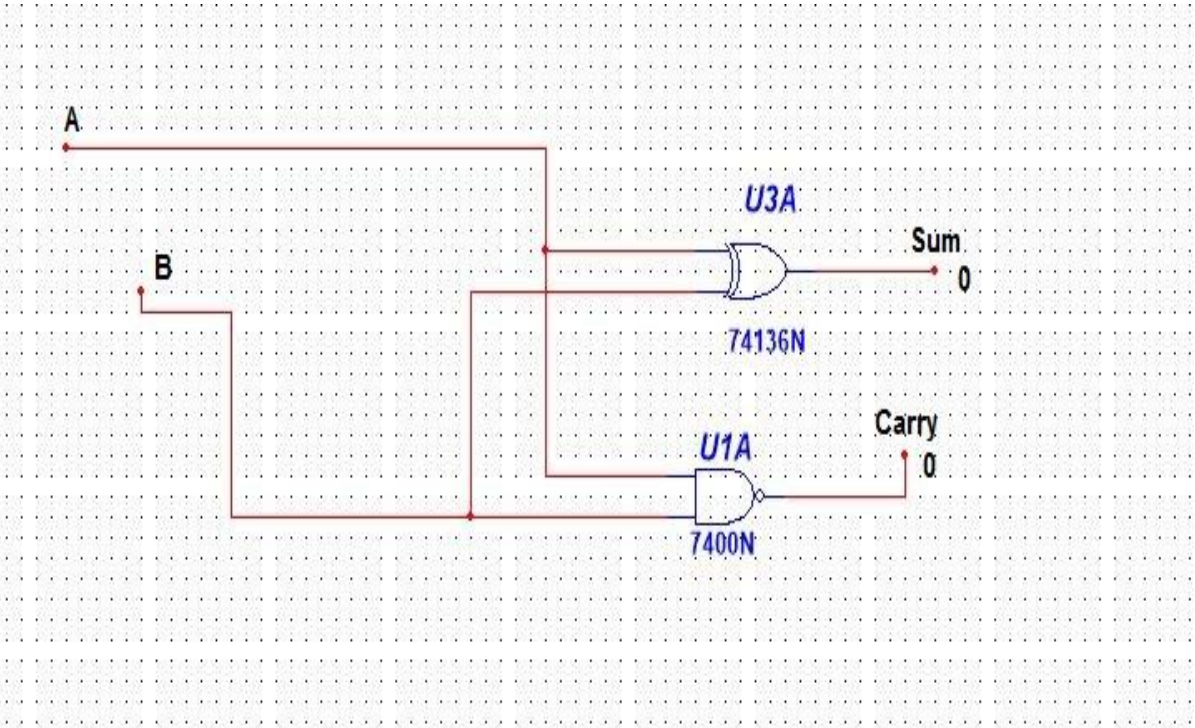
Note: Use MultiSim to design the follwing circuits. Use truth tables where necessary.

Q.1Design and verify the logic circuit for the following:
(a)Half adder using logic gates

Half Adder

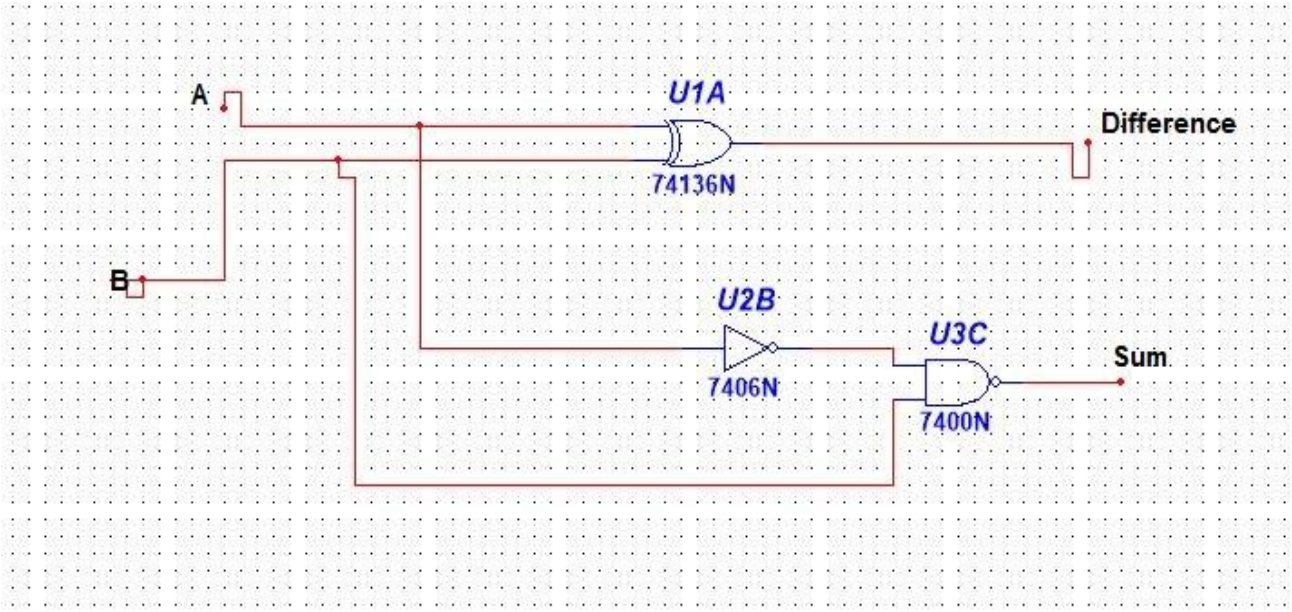
INPUTS		OUTPUTS	
A	**B**	**SUM**	**CARRY**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

From the equation, it is clear that this 1-bit adder can be easily implemented with the help of EXOR Gate for the output 'SUM' and an AND Gate for the carry. Take a look at the implementation below.



(b) Half-subtractor using logic gate

The designing of half subtractor can be done by using logic gates like NAND gate & Ex-OR gate. In order to design this half subtractor circuit, we have to know the two concepts namely difference and borrow.



If we monitor cautiously, it is fairly clear that the variety of operation executed by this circuit which is accurately related to the EX-OR gate operation. Therefore, we can simply use the EX-OR gate for making difference. In the same way, the borrow produced by half adder circuit can be simply attained by using the blend of logic gates like AND- gate and NOT-gate.

Truth Table

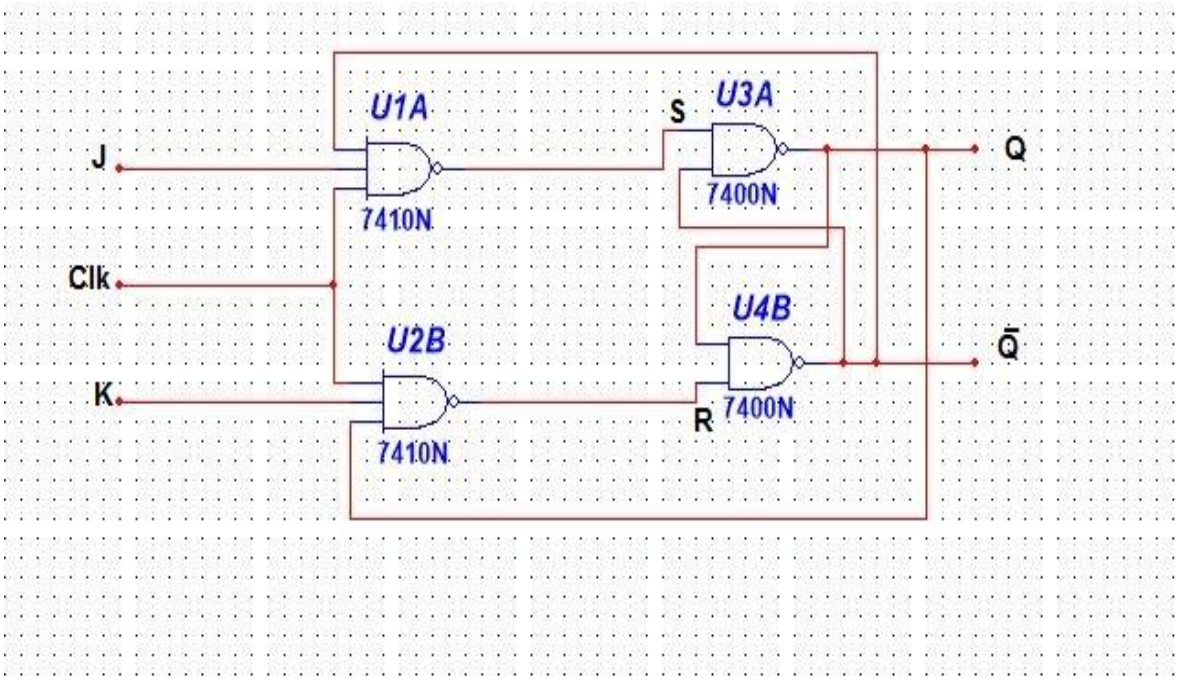
The half subtractor truth table explanation can be done by using the logic gates like EX-OR logic gate and AND gate operation followed by NOT gate.

First Bit	Second Bit	Difference (EX-OR Out)	Borrow (NAND Out)
0	0	0	0

1	0	1	0
0	1	1	1
1	1	0	0

(c) J K Flip flop

The **JK flip flop** is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level "1". Due to this additional clocked input, a JK flip-flop has four possible input combinations, "logic 1", "logic 0", "no change" and "toggle". The symbol for a JK flip flop is similar to that of an *SR Bistable Latch* as seen in the previous tutorial except for the addition of a clock input.

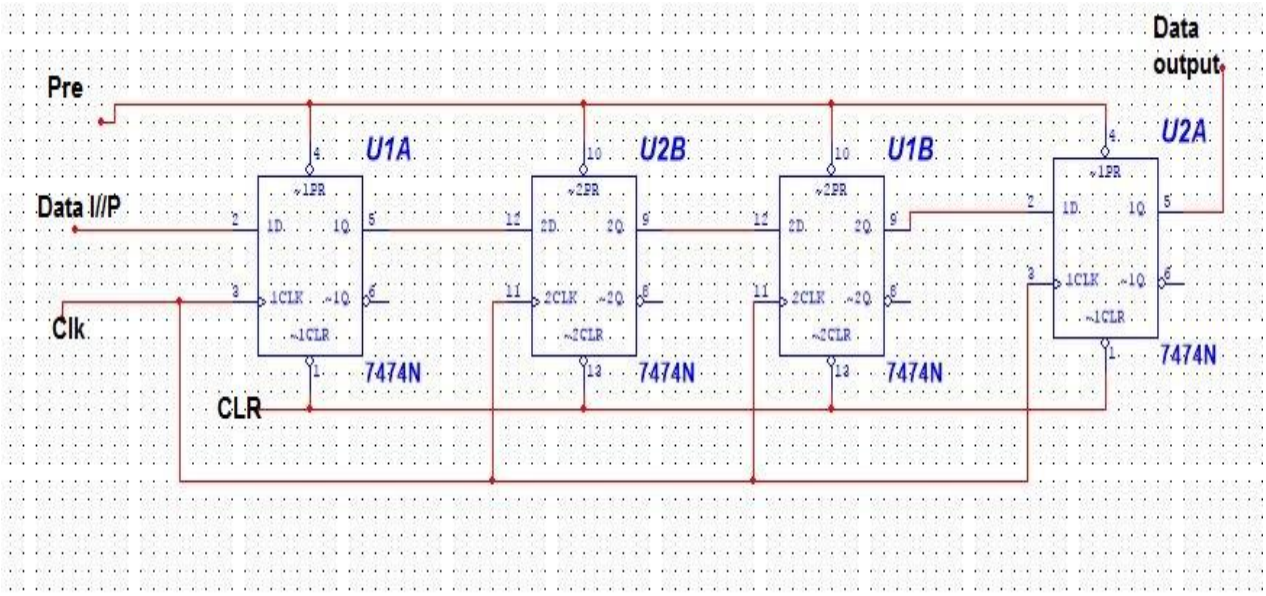


The Truth Table for the JK Function

	Clock	Input		Output		Description
	Clk	J	K	Q	Q	
same as for the Jk Latch	X	0	0	1	0	Memory no change
	X	0	0	0	1	
	¯↓_	0	1	1	0	Reset Q » 0
	X	0	1	0	1	
	¯↓_	1	0	0	1	Set Q » 1
	X	1	0	1	0	
toggle action	¯↓_	1	1	0	1	Toggle
	¯↓_	1	1	1	0	

(d) Serial in-serial Out shift register

The serial in/serial out shift register accepts data serially – that is, one bit at a time on a single line. It produces the stored information on its output also in serial form.



TRUTH TABLE:

CLK	Serial in	Serial out
1	1	0
2	0	0
3	0	0
4	1	1
5	X	0
6	X	0
7	X	1

E).synchronus BCD counter

This device is an Synchronous UP/DOWN (BCD) Decade Binary Counter. A LOW-to-HIGH transition on the clock input will advance the count by one.

The counter has an asynchronous parallel

load capability permitting the counter to be preset. When the $\overline{\text{LOAD}}$ is LOW, information present on the Parallel Data inputs (A,B,C,D) is loaded into the counter and appears on the outputs regardless of the conditions of the clock

inputs. A HIGH signal on the $\overline{\text{CTEN}}$ input inhibits counting. When $\overline{\text{CTEN}}$ is LOW, internal state change are initiated synchronously by the LOW-to-HIGH transition on the clock input. The direction of counting is determined by the $\overline{\text{U/D}}$ input signal as

indicated in the Mode selection table below.

Two types of outputs are provided as overflow/underflow indicators. The MAX/MIN output is normally LOW and goes HIGH when the counter reaches zero (LLLL) in the count-down mode or

reaches maximum (HLLH) in the count-up mode. The $\overline{RCO}$ output is normally HIGH but when $\overline{CTEN}$ is LOW and MAX/MIN is HIGH it will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again.

Mode selection table:

PL	$\overline{\text{CTEN}}$	$\overline{\text{U/D}}$	CLK	MODE
H	L	L	↑	COUNT UP
H	L	H	↑	COUNT DOWN
L	X	X	X	LOAD
H	H	X	X	HOLD

H = HIGH Level.
L = LOW Level.
X = Don't Care.
↑ = LOW-to-HIGH transition of the Clock input.

$\overline{\text{RCO}}$ Truth table:

$\overline{\text{CTEN}}$	MAX/MIN	CLK	MODE
L	H	⌊	L
H	X	X	H
X	L	X	H

H = HIGH Level.
L = LOW Level.
X = Don't Care.