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**Reg No. 16550**

**Mid term Assignment: No 1**

**Subject: Digital logic design**

**(Lab)**

**Instructor : Muhammad Amin**

# Lab : 1

Table 1.1 Output Observation Table

S.No	Inputs		Outputs							
	A	B	Not		AND	OR	NAND	NOR	XOR	XNOR
			A	B						
1	0	0	1	1	0	0	1	1	0	1
2	0	1	1	0	0	1	1	0	1	0
3	1	0	0	1	0	1	1	0	1	0
4	1	1	0	0	1	1	0	0	0	1

out