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I.D :

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Subject :

DLD

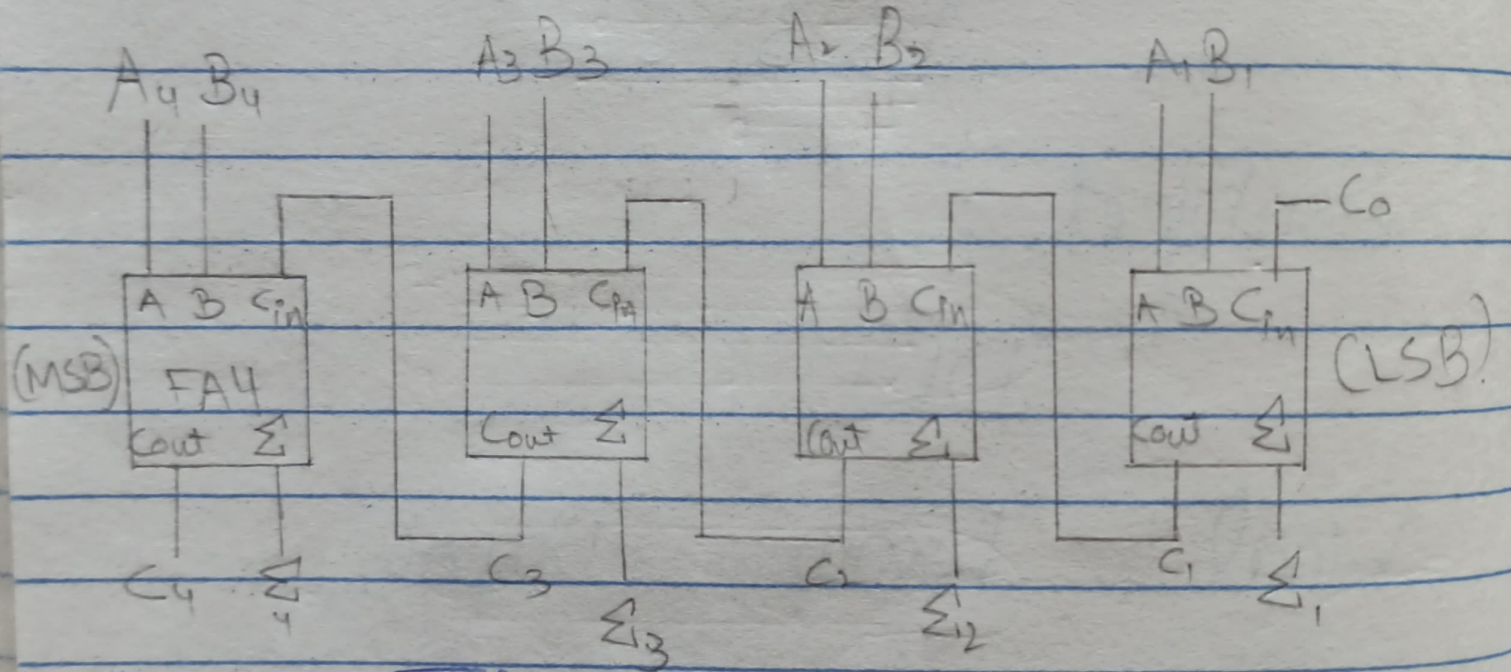
Final Exam Paper

Teacher :

Sir Amin

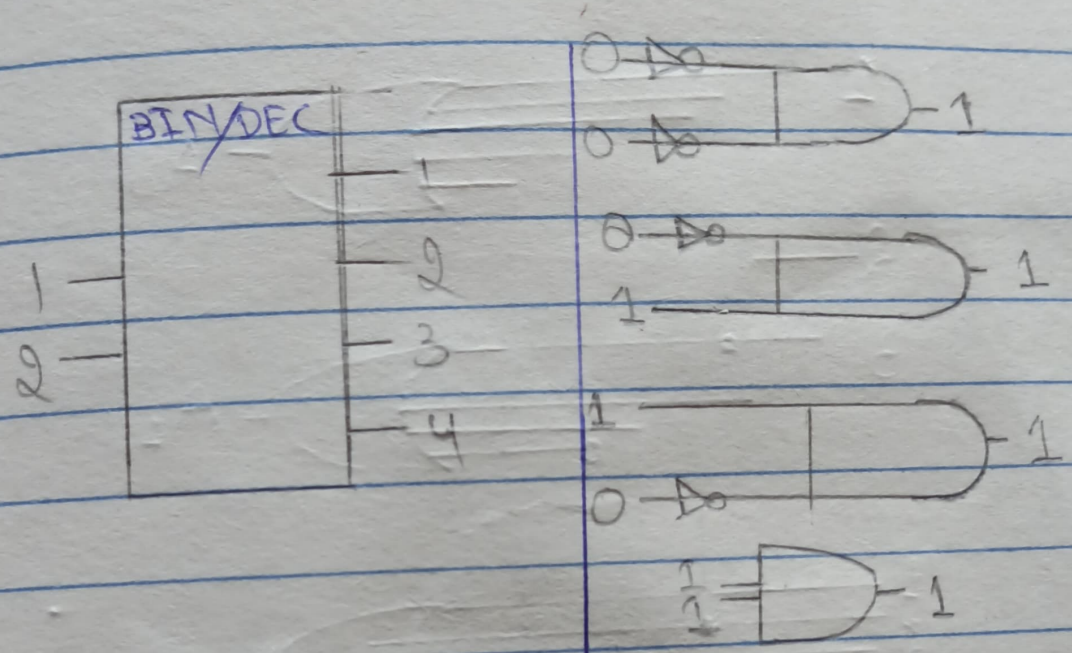
Q1: Draw and explain the logic diagram for each of the following:

a) A circuit for adding or subtracting two 4-bit numbers.



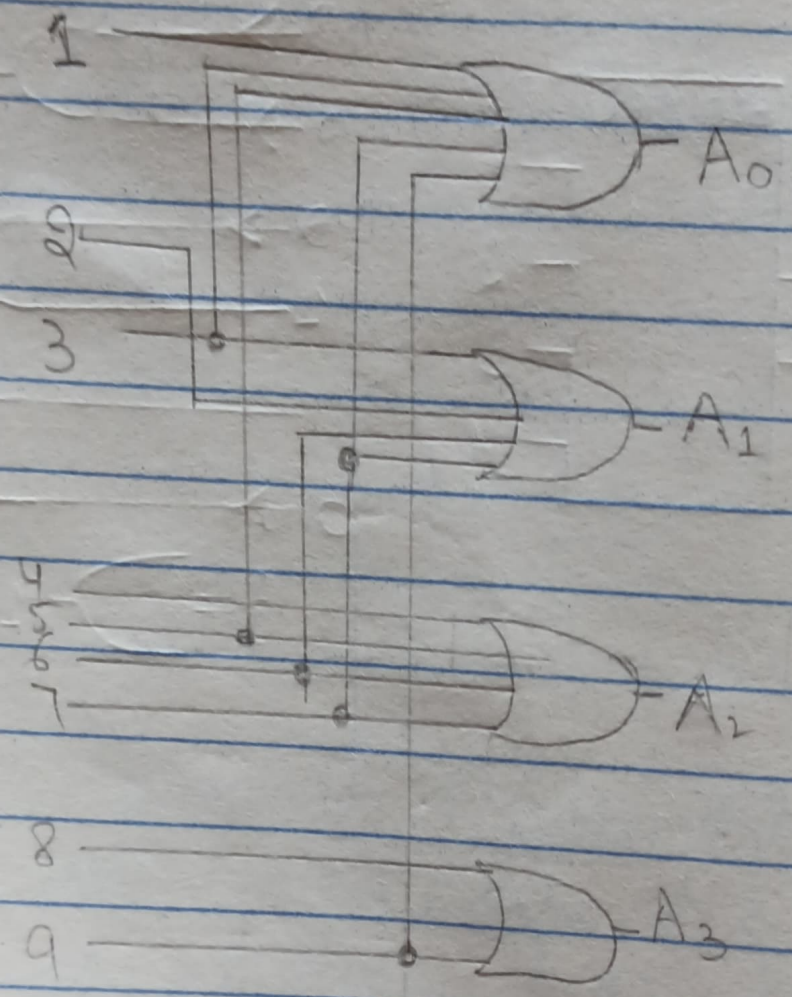
Explanation: Following diagram is the 4 bit parallel adder. 4 bits are entered and the result outcome is the sum of all the 4 bits.

Q1 : part b : D : 4 bit active low decoder.



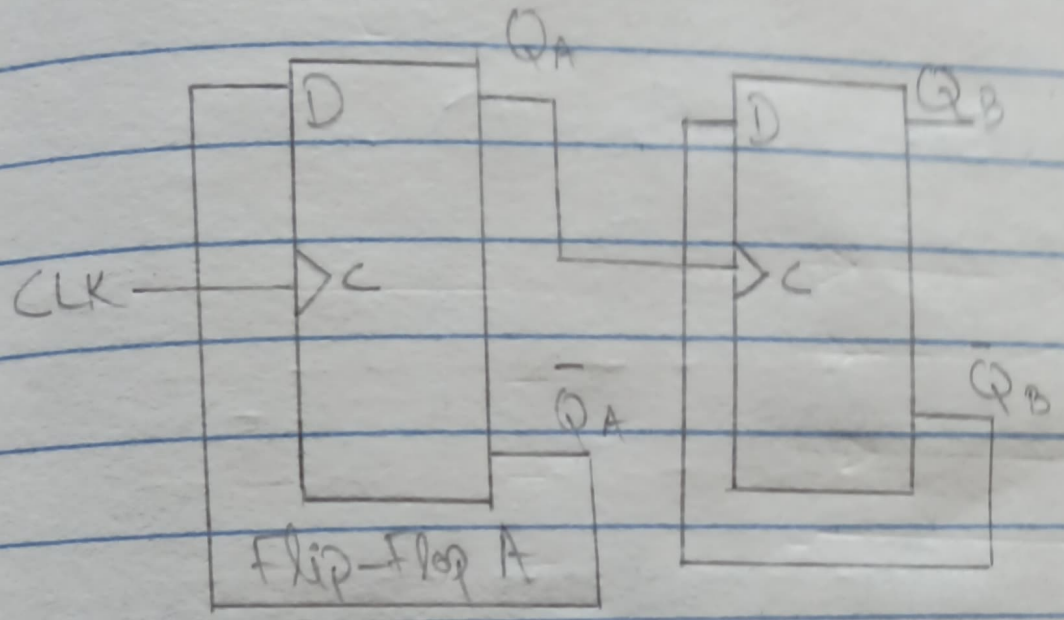
The following diagram is a 4-bit decoder. Bits are decoded and output is given in $D_3 D_2 D_1 D_0$.

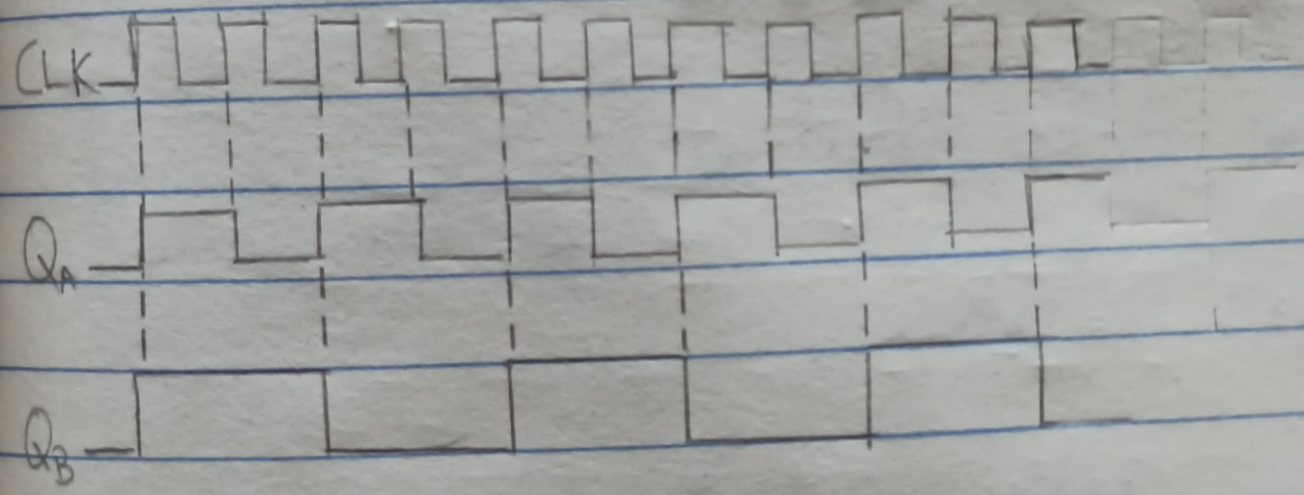
Q2 G1: part :C : Decimal to BCD Encoder.



Explanation: The basic operation the circuit is as follows. When a HIGH appears on one the decimal digit input lines, the approximate levels occur on the four BCD output lines.

Q: 1 : part : D :





Explanation:

These two D-flip flops are used to divide the clock frequency by 4. Q_A is one-half the frequency and Q_B is one-fourth the frequency of CLK.

Q:2 : Part : a :

a) $S_0 = 1$, $S_1 = 0$.
b) $S_0 = 0$, $S_1 = 1$
c) $S_0 = 1$, $S_1 = 1$
d) $S_0 = 0$, $S_1 = 1$.

-> The data output is equal to D_0 only if $S_1 = 0$ and $S_0 = 0$: $Y = D_0 \bar{S}_1 \bar{S}_0$

=> The data output is equal to D_1 only if $S_1 = 0$ and $S_0 = 1$: $Y = D_1 \bar{S}_1 S_0$

=> The data output is equal to D_2 only if $S_1 = 1$ and $S_0 = 0$: $Y = D_2 S_1 \bar{S}_0$

=> The data out is equal to D_3 only if $S_1 = 1$ and $S_0 = 1$: $Y = D_3 S_1 S_0$.

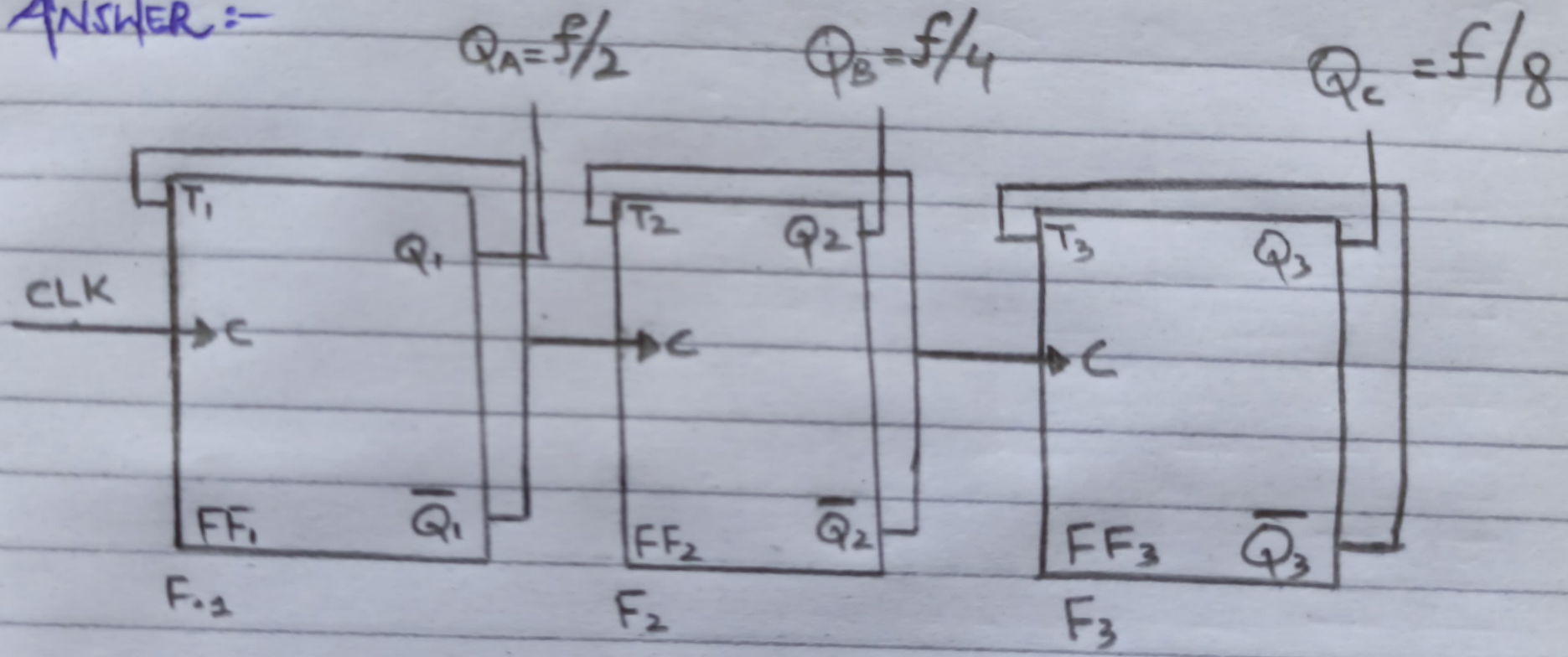
The total expression for data output is:

$$Y = D_0 \bar{S}_1 \bar{S}_0 + D_1 \bar{S}_1 S_0 + D_2 S_1 \bar{S}_0 + D_3 S_1 S_0.$$

The implementation of this equation requires four 3-input AND gates, a 4-input OR gate, and two inverters to generate the complements of S_1 and S_0.

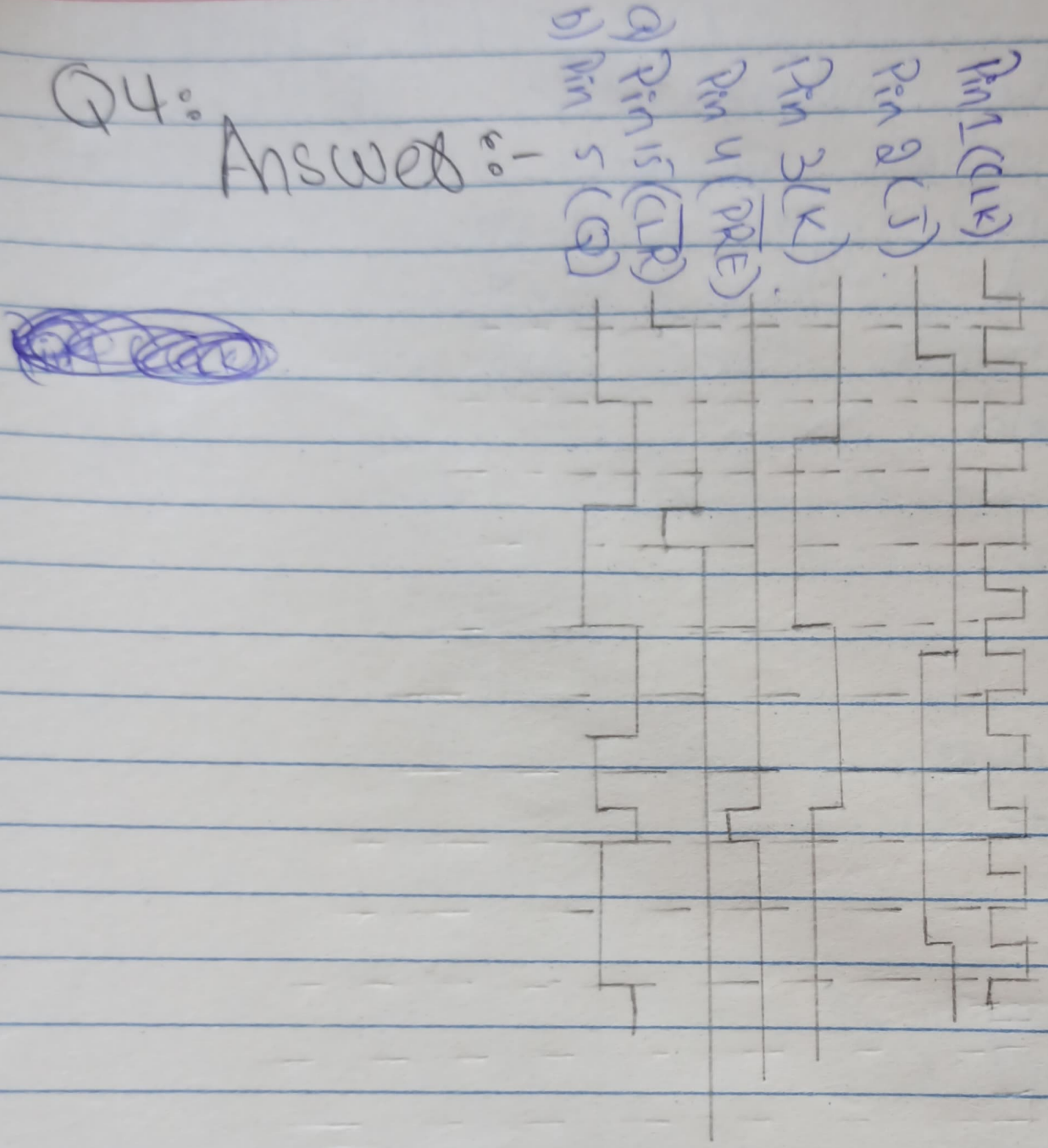
Q3:-

ANSWER:-


$Q_A = f/2$
$Q_B = f/4$
$Q_C = f/8$
CLK
T_1
Q_1
C
FF_1
$\overline{Q}_1$
F_1
T_2
Q_2
C
FF_2
$\overline{Q}_2$
F_2
T_3
Q_3
C
FF_3
$\overline{Q}_3$
F_3

Q4:

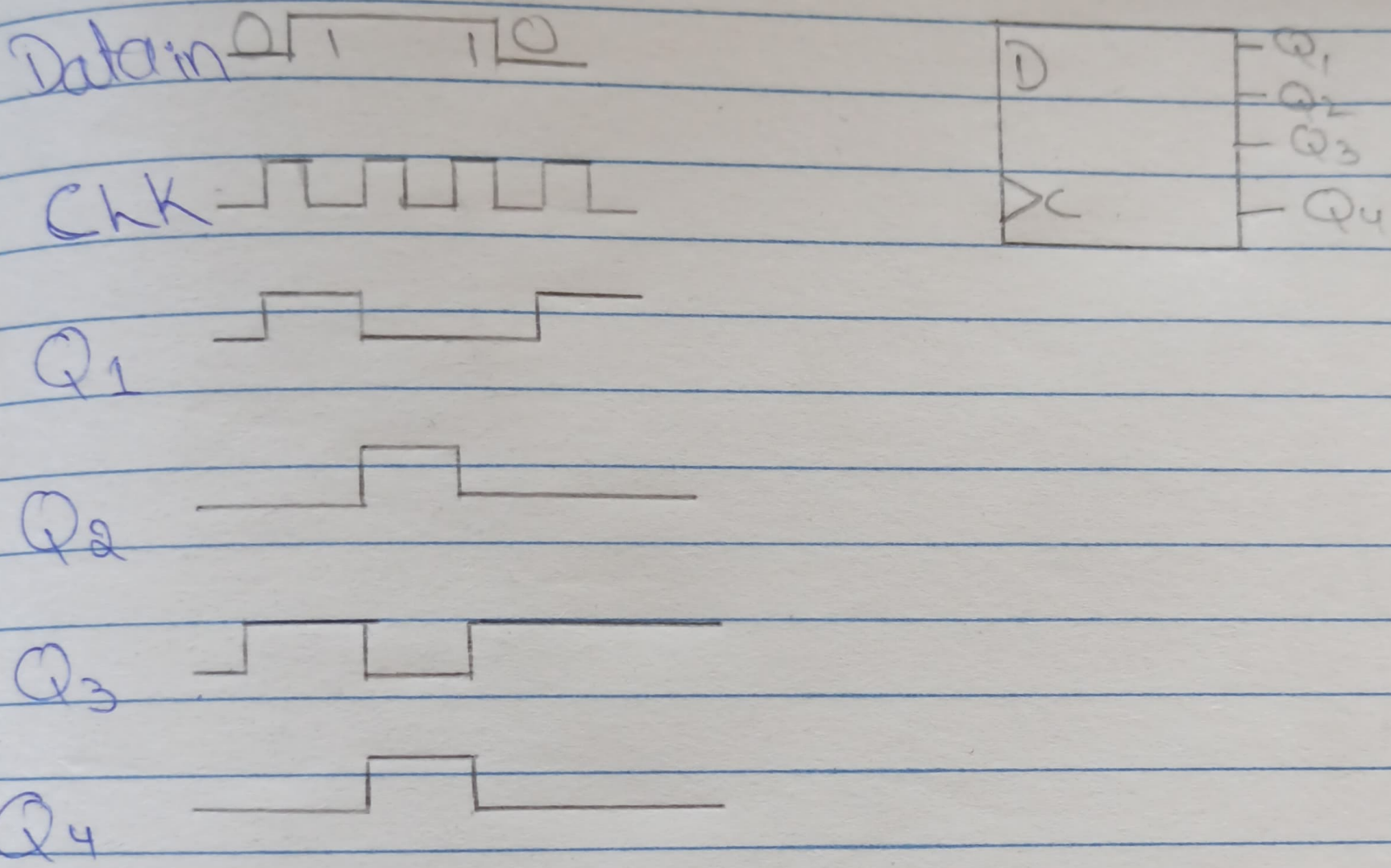
Answer:-



The resulting 'Q' waveform is shown in the above figure. Each time a low is applied to the PRE or $\overline{CLR}$, the flip flop is set or reset the Q regardless of the state of the other inputs.

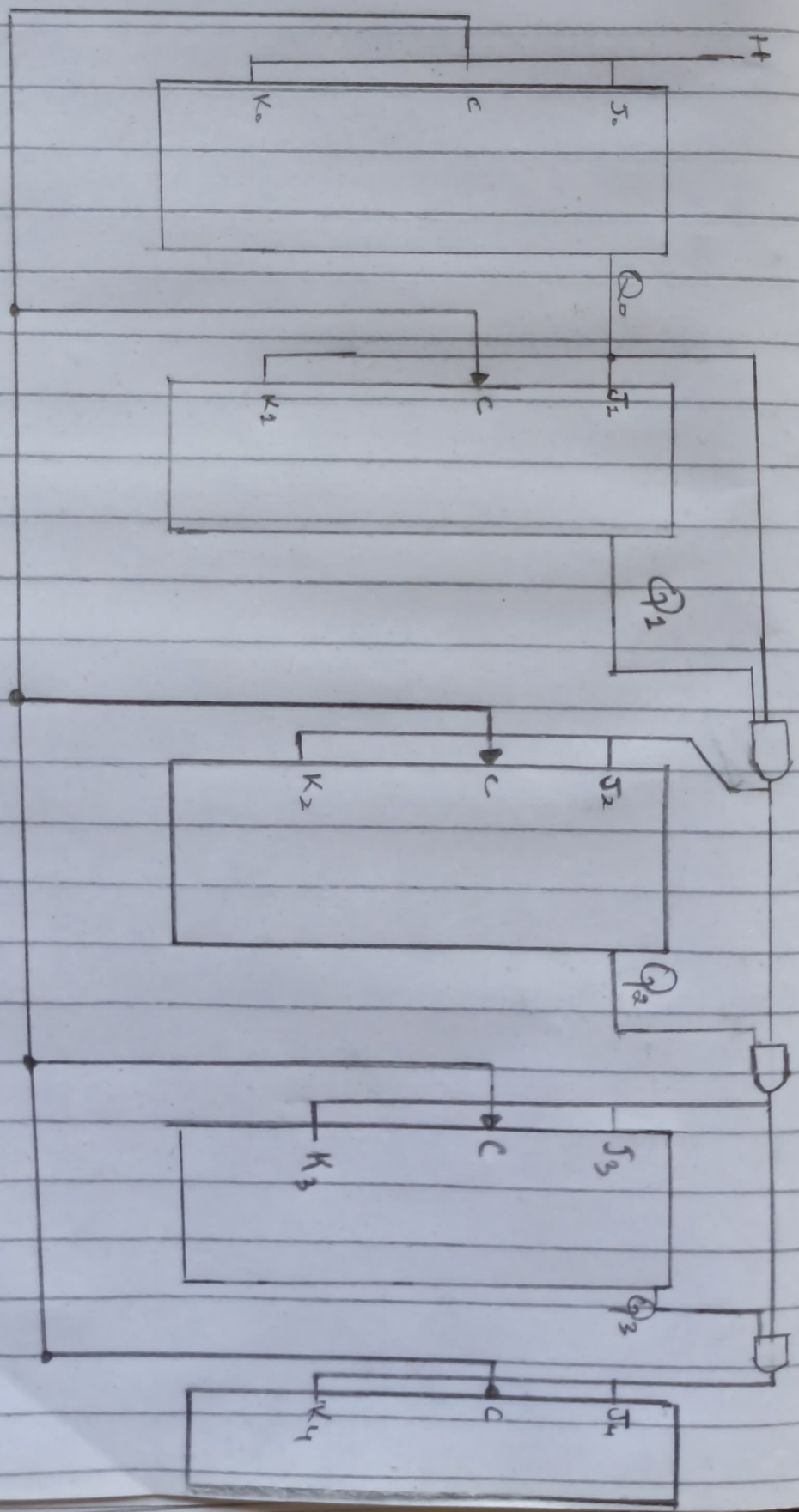
Q5:

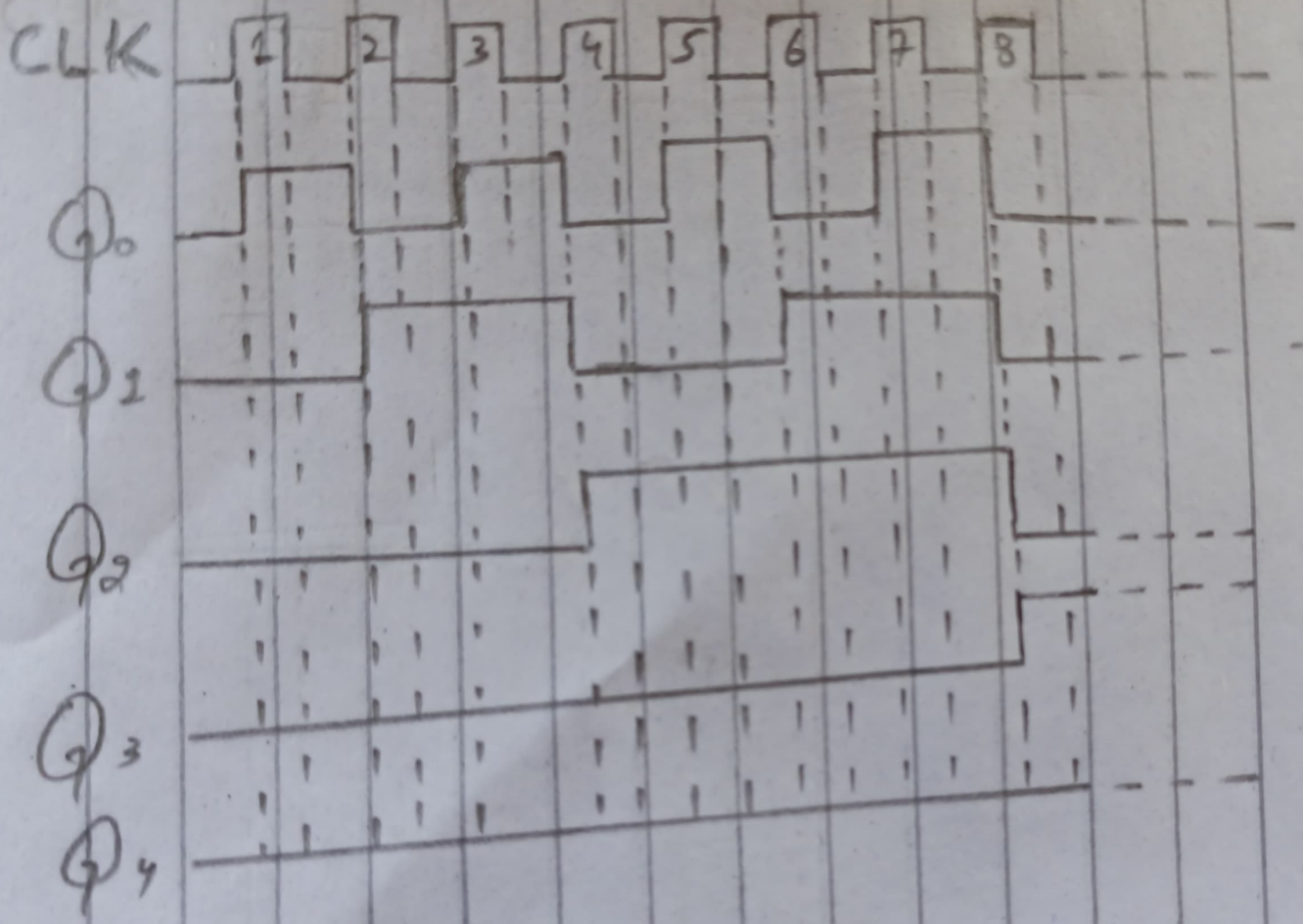
Answer:



Q: 6:

ANSWER:-




CLK
1
2
3
4
5
6
7
8
Q0
Q1
Q2
Q3
Q4