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Reg# 16549

Semester: 6th

Major Assignment: DLD Final Term

Submitted to: Sir Muhammad Amin

Q:(a) Draw Circuit for adding or subtracting two 4 bits number

Control Input (M)
For Adding we Input 0 in Control Input

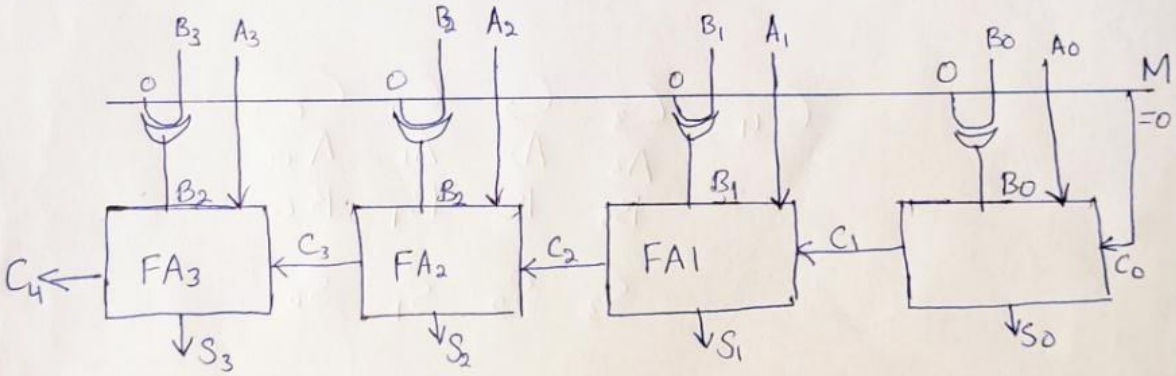
Adder

$A \oplus 0 = B$
$A \oplus 1 = B'$
$A - B = (A + B' + 1)$

For Adding M=0 (A+B) add

C_4 C_3 C_2 C_1 C_0
A_3 A_2 A_1 A_0 (A) } Two
B_3 B_2 B_1 B_0 (B) }

S_3 S_2 S_1 S_0



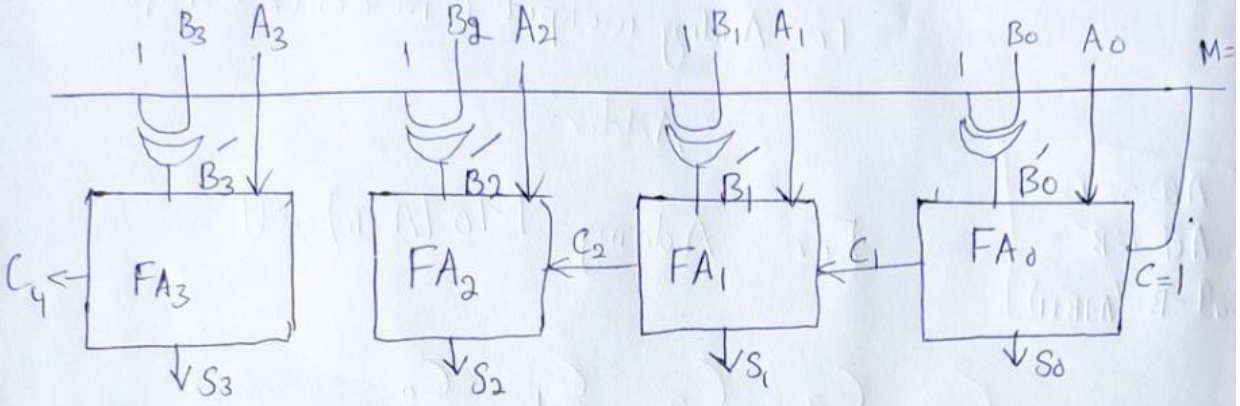
Intial Carry = 0 because for adder we input 0

Final Output is equal to C_4

For Subtractor input will be 1

$A \oplus 0 = A$

So $M = 1$



$A - B = (A + B' + 1)$

$M = 1$ $(A - B)$ Subtract

C_4	C_3	C_2	C_1	C_0
	A_3	A_2	A_1	A_0
	B_3	B_2	B_1	B_0
	S_3	S_2	S_1	S_0

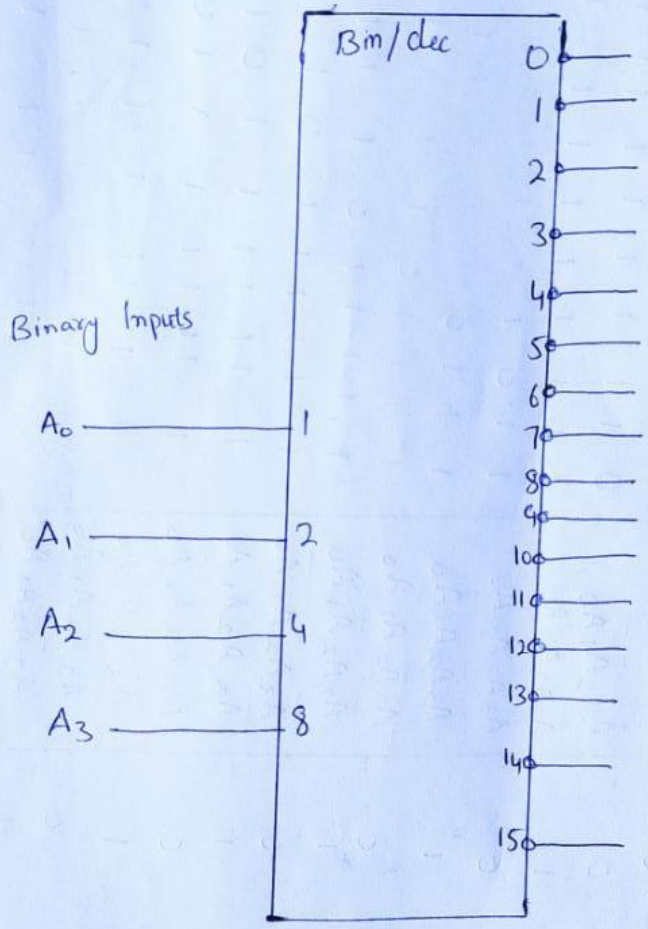
if we 1001 (9)
-0111 (7)
0010 (2)

it will be subtractor if Input is 1

(b) Draw a circuit of 4-bit active low decoder

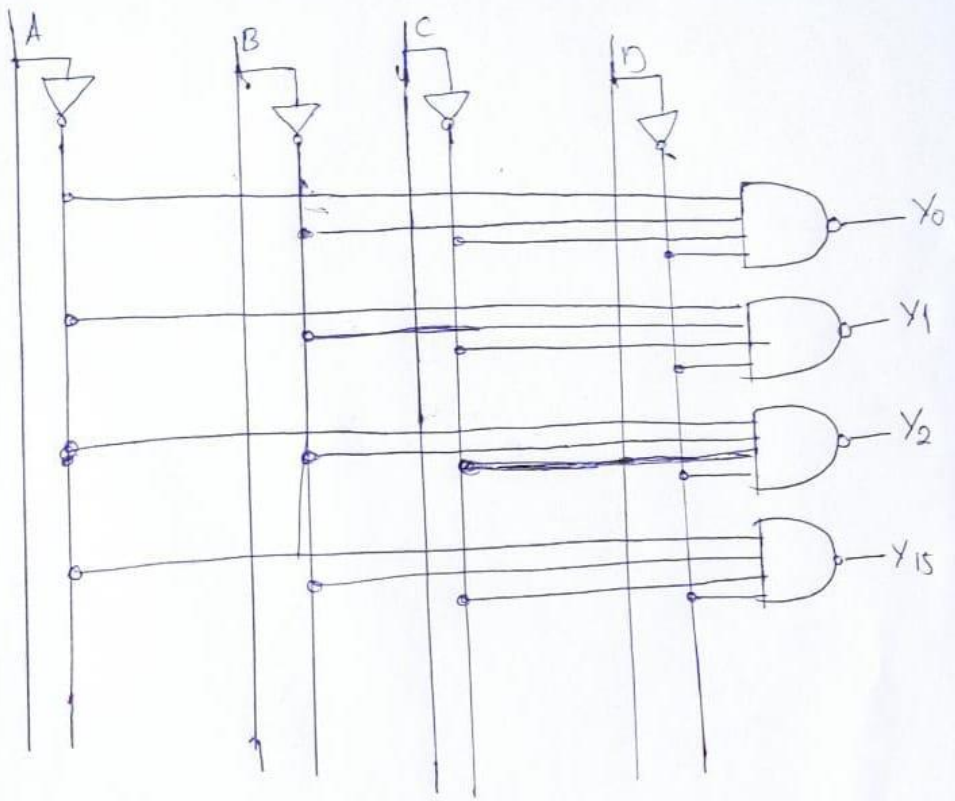
4-bit Decoder for Active low

Binary Inputs A_0, A_1, A_2, A_3



In an ~~acto~~ active-low output is required for each decoded number, the entire decoder can be implemented with NAND gates & inverters.

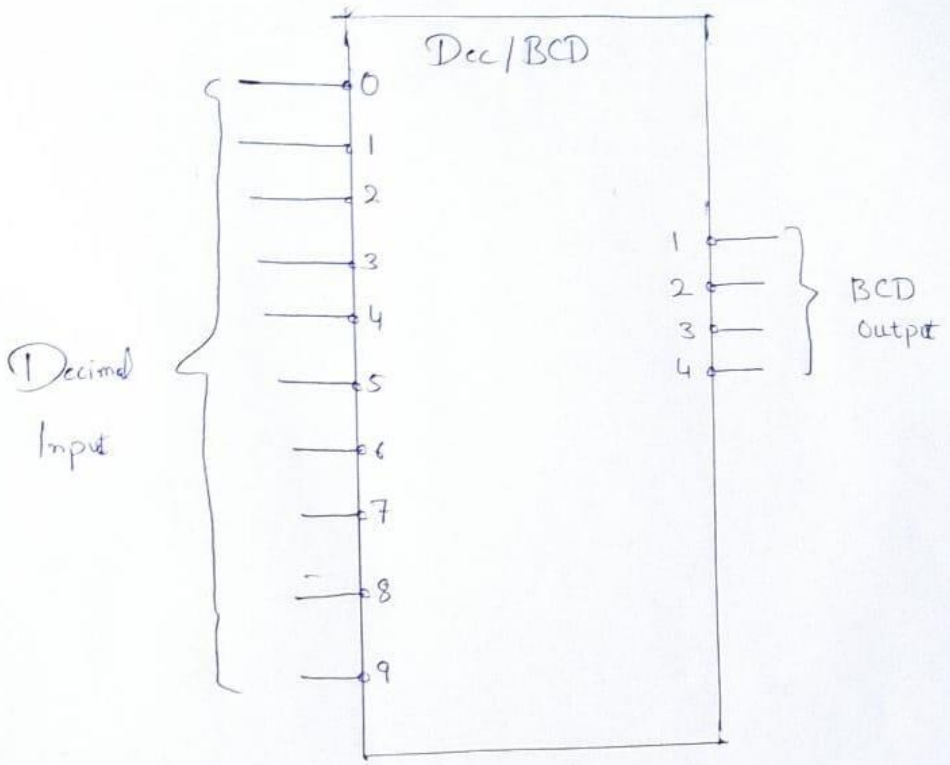
(b) Circuit of 4-bit active low



Decoding functions & truth table for 4-bit active-Low decoder Outputs

Decimal Digit	Binary Inputs A_3	A_2	A_1	A_0	Decoding Function	Outputs 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	$\bar{A}_3\bar{A}_2\bar{A}_1\bar{A}_0$	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	$\bar{A}_3\bar{A}_2\bar{A}_1 A_0$	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	0	1	0	$\bar{A}_3\bar{A}_2 A_1\bar{A}_0$	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
3	0	0	1	1	$\bar{A}_3\bar{A}_2 A_1 A_0$	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
4	0	1	0	0	$\bar{A}_3 A_2\bar{A}_1\bar{A}_0$	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
5	0	1	0	1	$\bar{A}_3 A_2\bar{A}_1 A_0$	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
6	0	1	1	0	$\bar{A}_3 A_2 A_1\bar{A}_0$	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
7	0	1	1	1	$\bar{A}_3 A_2 A_1 A_0$	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
8	1	0	0	0	$A_3\bar{A}_2\bar{A}_1\bar{A}_0$	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
9	1	0	0	1	$A_3\bar{A}_2\bar{A}_1 A_0$	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
10	1	0	1	0	$A_3\bar{A}_2 A_1\bar{A}_0$	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
11	1	0	1	1	$A_3\bar{A}_2 A_1 A_0$	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
12	1	1	0	0	$A_3 A_2\bar{A}_1\bar{A}_0$	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
13	1	1	0	1	$A_3 A_2\bar{A}_1 A_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
14	1	1	1	0	$A_3 A_2 A_1\bar{A}_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
15	1	1	1	1	$A_3 A_2 A_1 A_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

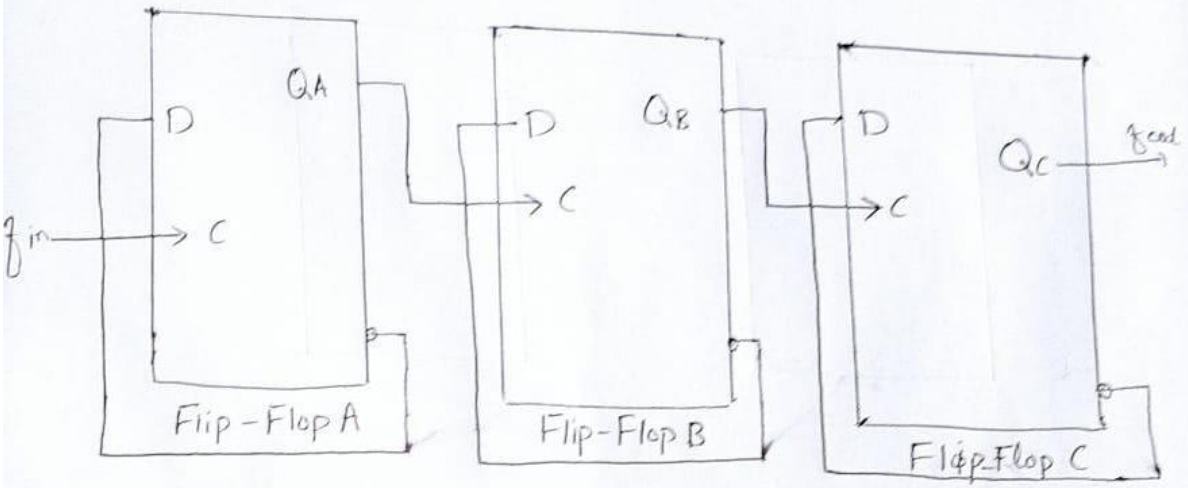
(c) Logic Diagram of ~~BCD to~~ decimal to BCD encoder



Truth Table

Decimal Digit	BCD CODE A_3	A_2	A_1	A_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

(d) Frequency divider / Use 3-JK flip flop & assume 16 KHZ frequency of the initial wave form



Q2: For the 4-Input multiplexer, data inputs are given as

$D = 0,\ D_1 = 1,\ D_2 = 0,\ D = 1$

Find the Output Y if the select inputs are given as

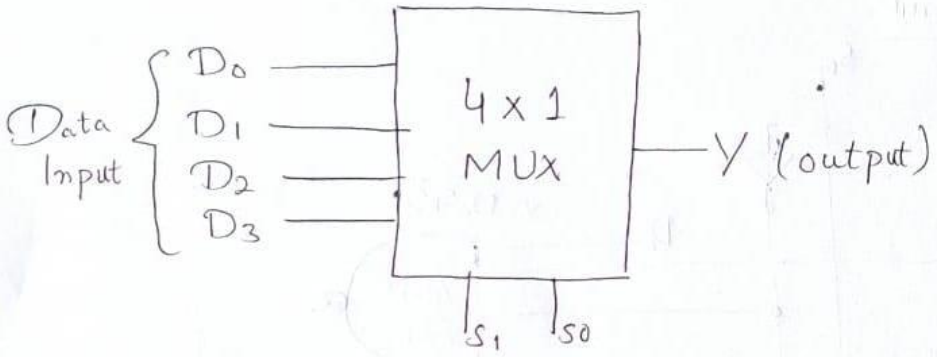
a) $S_0 = 1,\ S_1 = 0$

$S_0 = 0,\ S_1 = 1$

$S_0 = 1,\ S_1 = 1$

$S_0 = 0,\ S_1 = 0$

Answer:



Find Select lines:-

$n = 4$

$m = \log_2 n$

$m = \log_2 4$

$= \log_2 2^2 \quad \because \log_a a = 1$

$m = 2 \log_2 2 \quad 1 = 2 \cdot 1 = 2 \longrightarrow$ Select lines

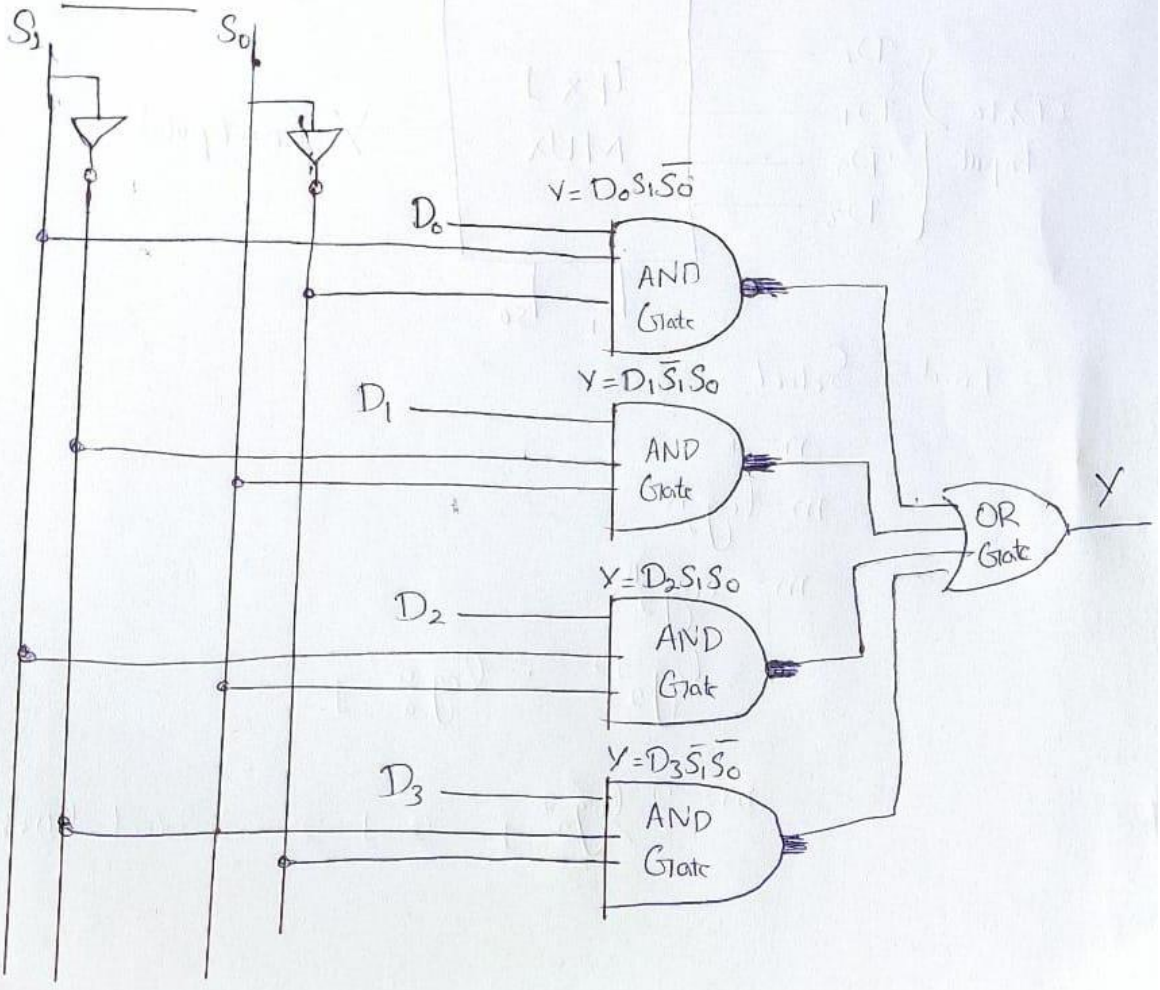
S_0	S_1	Data
1	0	D_0
0	1	D_1
1	1	D_2
0	0	D_3

Output (Y)

$Y = D_0 S_1 \bar{S}_0 + D_1 \bar{S}_1 S_0 + D_2 S_1 S_0 + D_3 \bar{S}_1 \bar{S}_0$

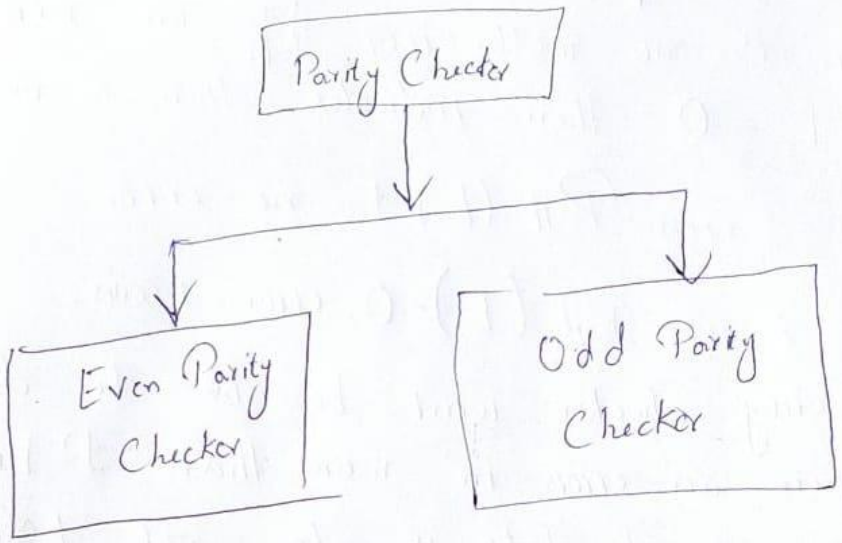
OutPut = $Y = D_0 S_1 \bar{S}_0 + D_1 \bar{S}_1 S_0 + D_2 S_1 S_0 + D_3 \bar{S}_1 \bar{S}_0$

Circuit



Q3- Timing diagram in Figure 01 shows input to a 9-bit parity checker. Draw the Σ Even & Σ odd output for the even parity checker

Answer- Parity Check: The combinational circuit at the receiver is the parity checker. This checker takes the recieved message including the parity bit as input. It gives output '1' if there is some error found & gives Output '0' if no error is found in the message including the Parity bit.



Even Parity Checker :- In Even Parity checker if the error bit (E) is equal to '1', then we have an error bit E=0 then indicates there is no error.

Error Bit (E) = 1, error occurs

Error Bit (E) = 0, no error

Odd Parity Checker:

In odd parity checker if an error bit (E) is equal to '1', then it indicates there is no ~~matter~~ error. If an error bit E = 0 then indicates there is an error

Error Bit (E) = 1, no error

Error Bit (E) = 0, error occurs.

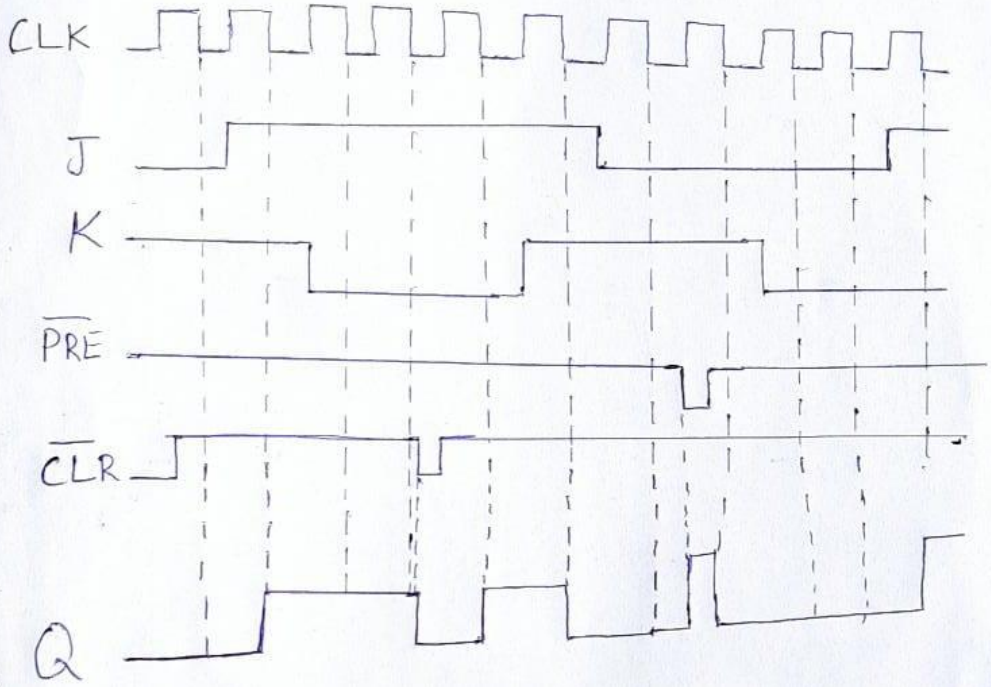
The parity checker won't be able to detect if there are errors in more than '1' bit & the correct of data is also not possible, these are the main disadvantages of the parity Checker.

The below table shows the truth table for the even parity checker in which PEC=1 if the error occurs, i.e, if odd number of 1s & PEC=0 if no error.

A	B	C	P	Parity error check C_P
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Q4- The waveforms in Figure 02 are appled to the J, K, CLK, $\overline{PRE}$, & $\overline{CLR}$ inputs as indicated. Determine the Q output, if the flip-flop is Initially Reset.

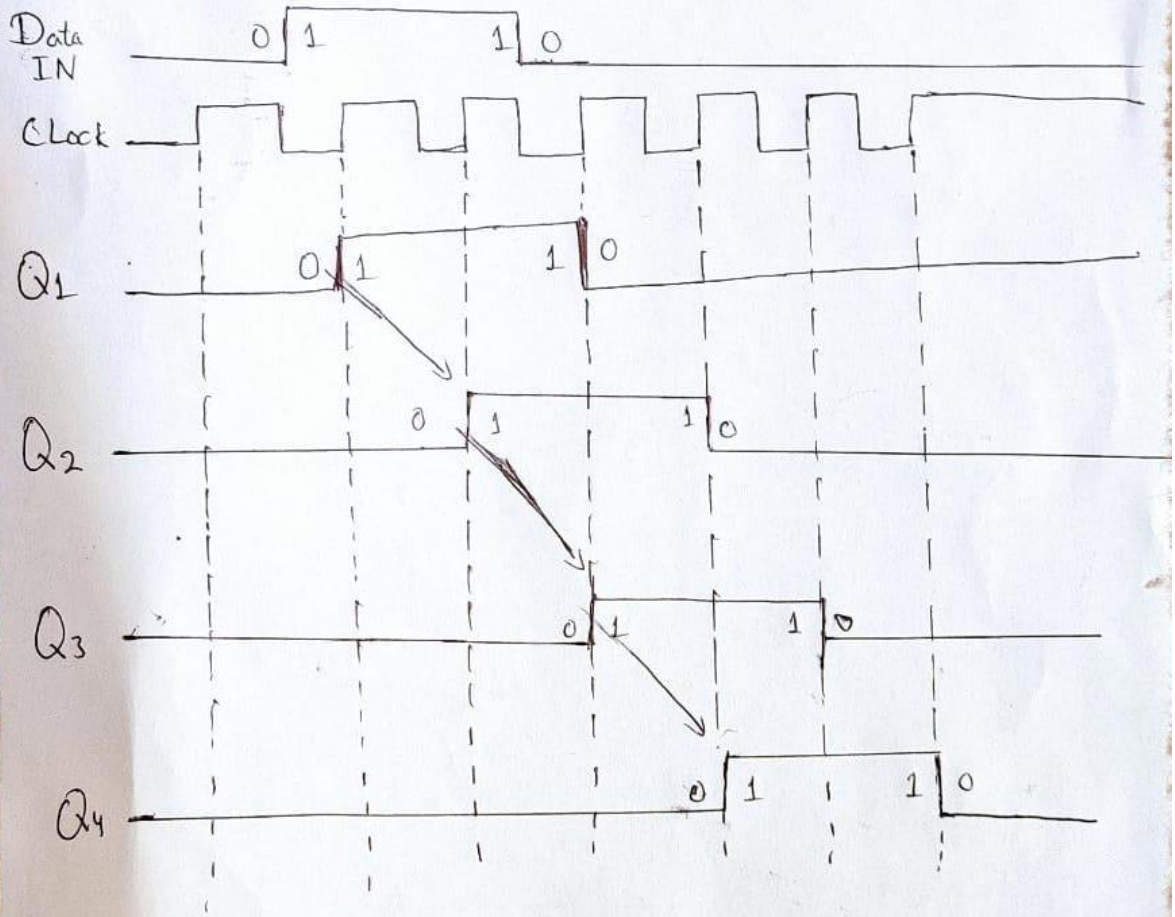
Answer:



Q5:- Use the waveforms in Figure 03 to draw the timing diagram for the parallel outputs (Q_1, Q_2, Q_3, Q_4) for the Shift register. Assume that register is initially cleared.

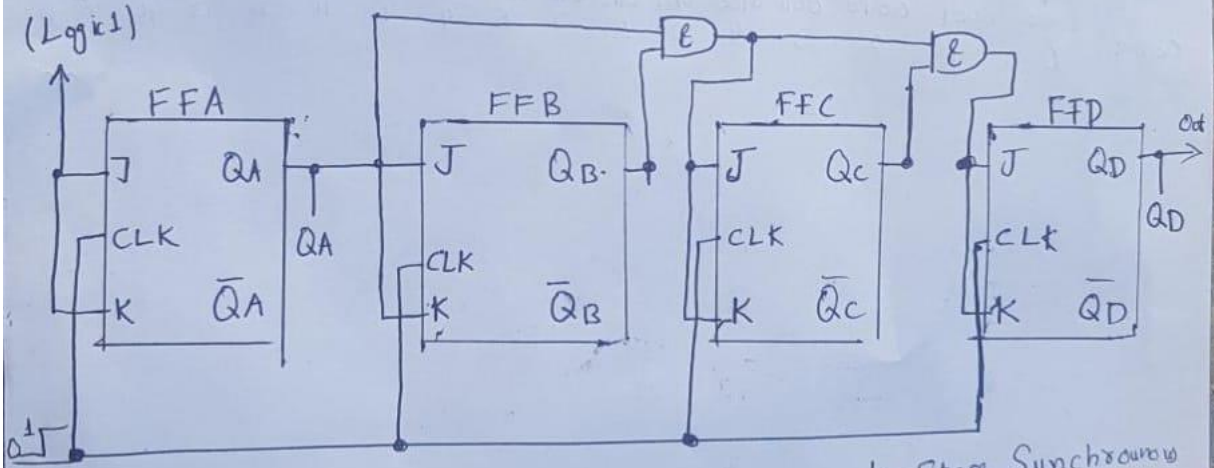
Ans:- Diagram:-

is Below:-



Q6:- Draw the logic diagram & timing diagram for the 4-bit stage Synchronous binary Counter. Verify that the waveforms of the Q outputs represent the Proper binary number after each clock pulse.

Ans:- Logic Diagram of 4 Stage Synchronous



4-Stage Synchronous binary Counter

4- Stage Synchronous Counter Waveform Timing Diagram