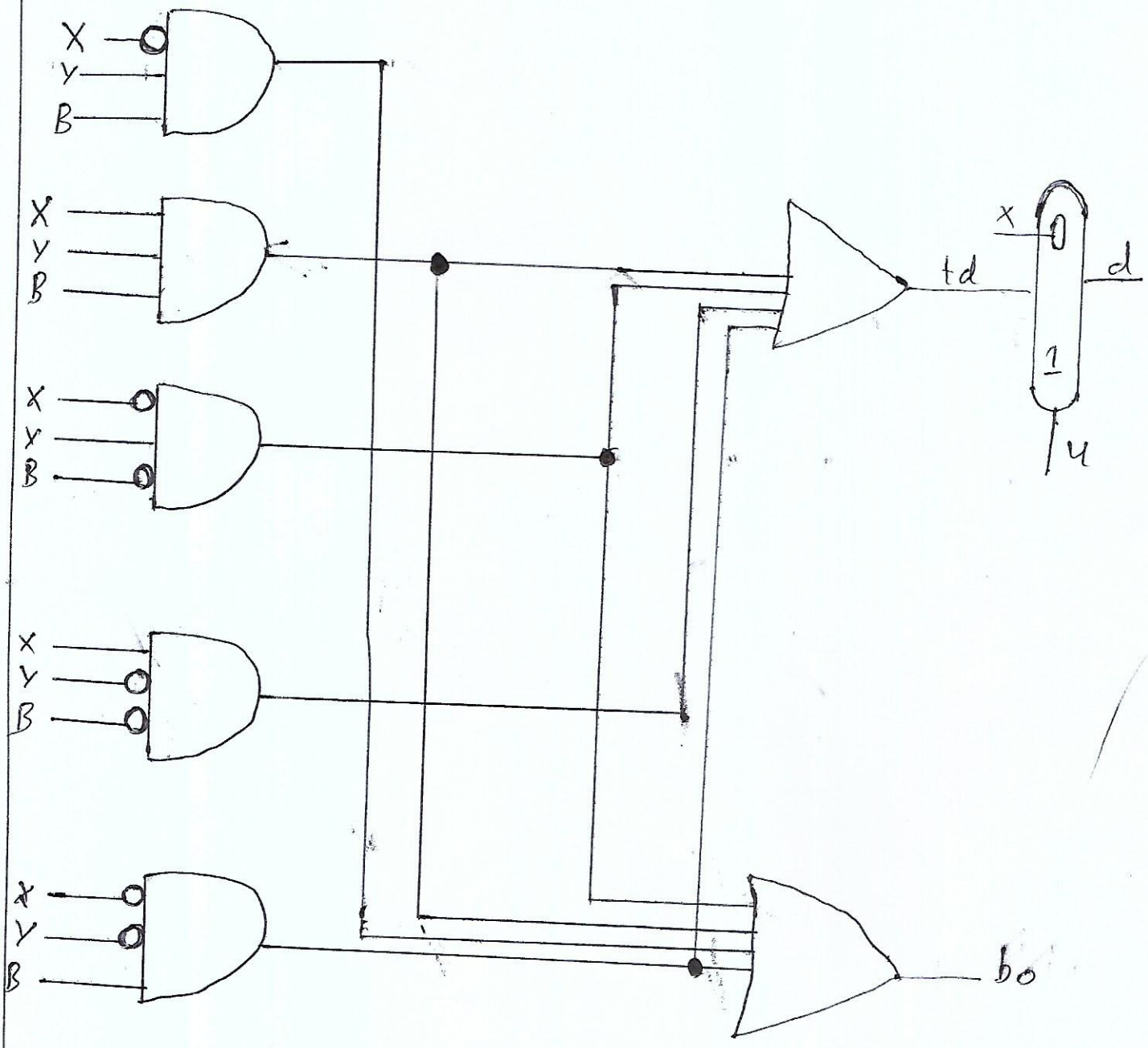
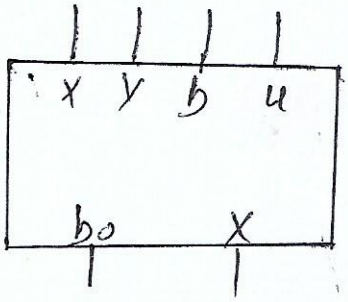
DLD Assignment

Name: M.Abbas 13063 BSSE-B

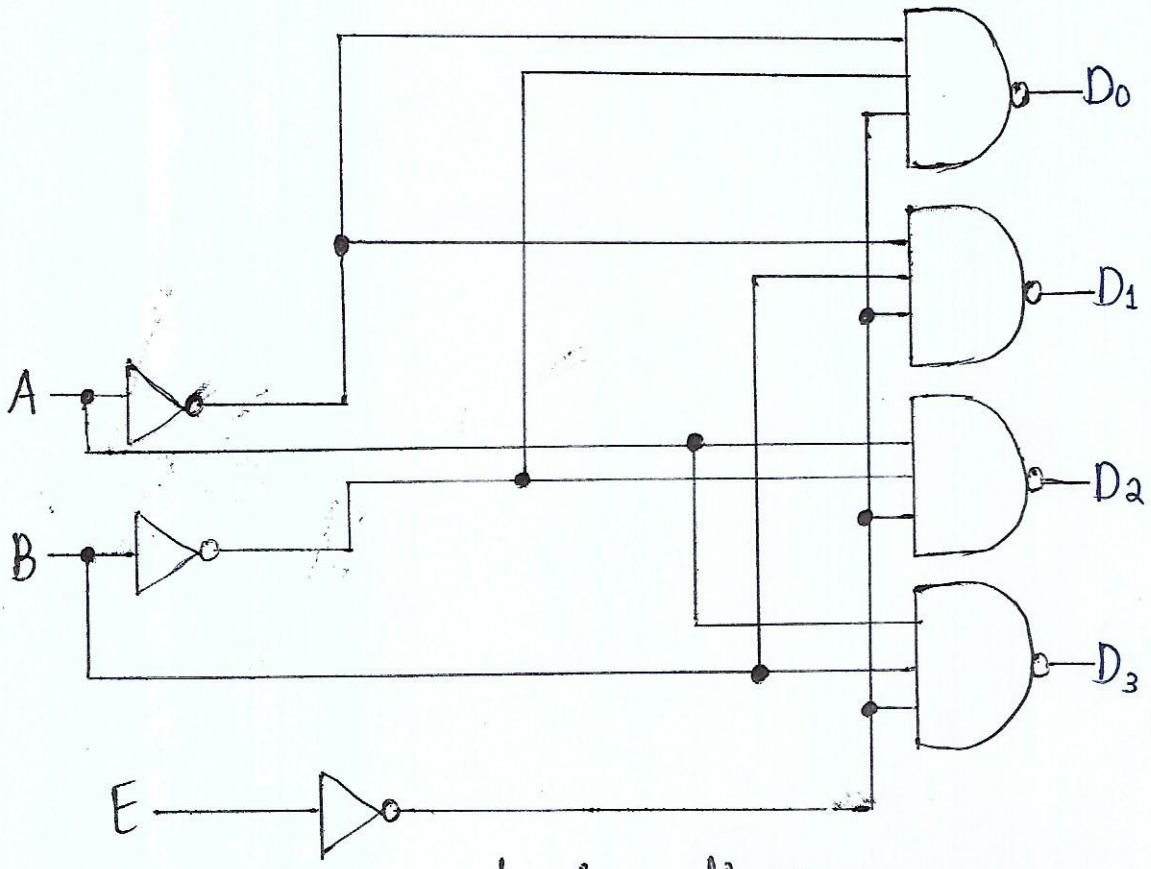
Q1 (A) A circuit for adding or subracting two numbers.





Q1 (B)

4-bit active low decorder



Logic diagram

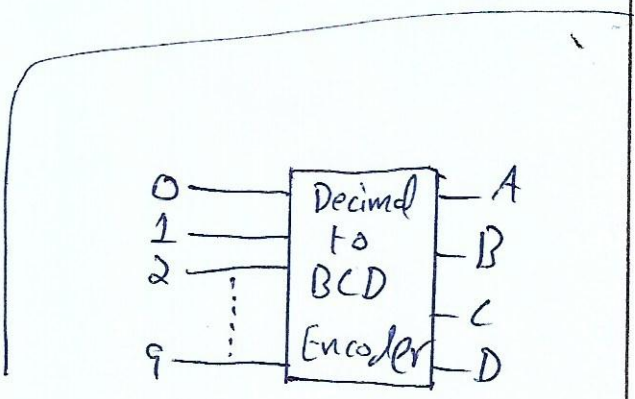
E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

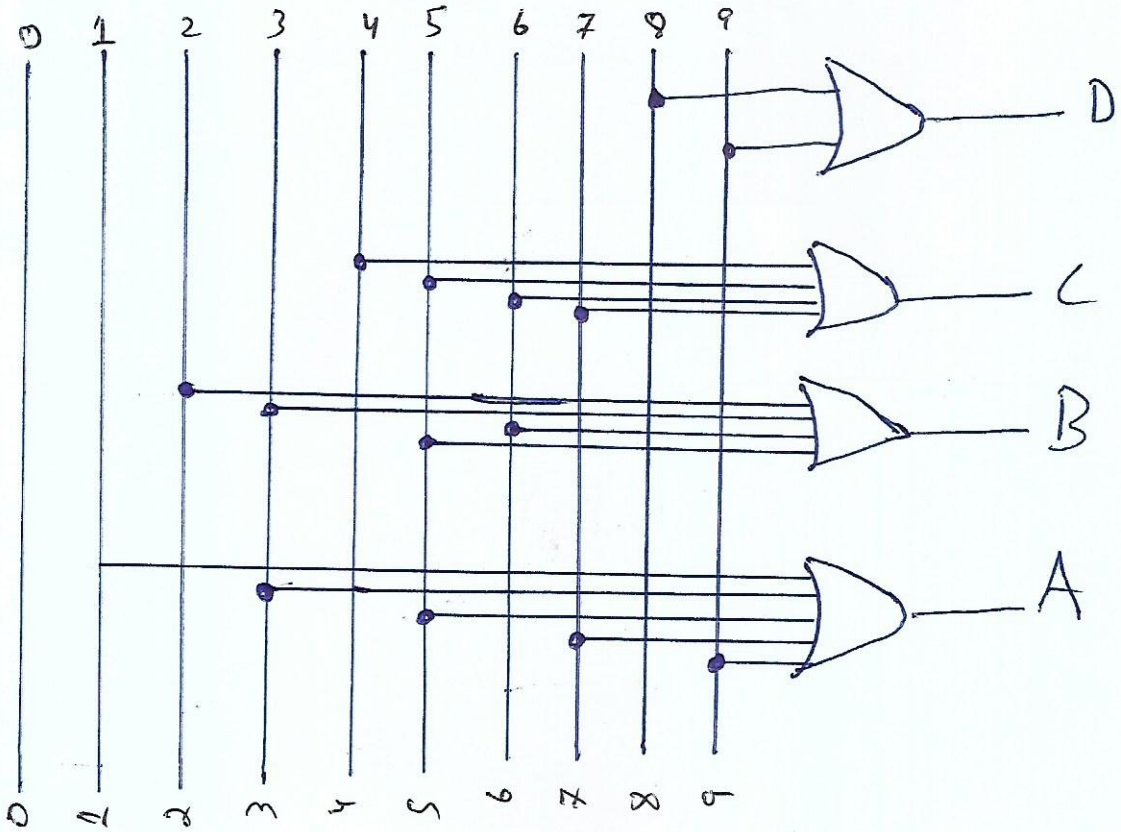
(b) Truth table

Q1
Part: C

Decimal to BCD Encoder

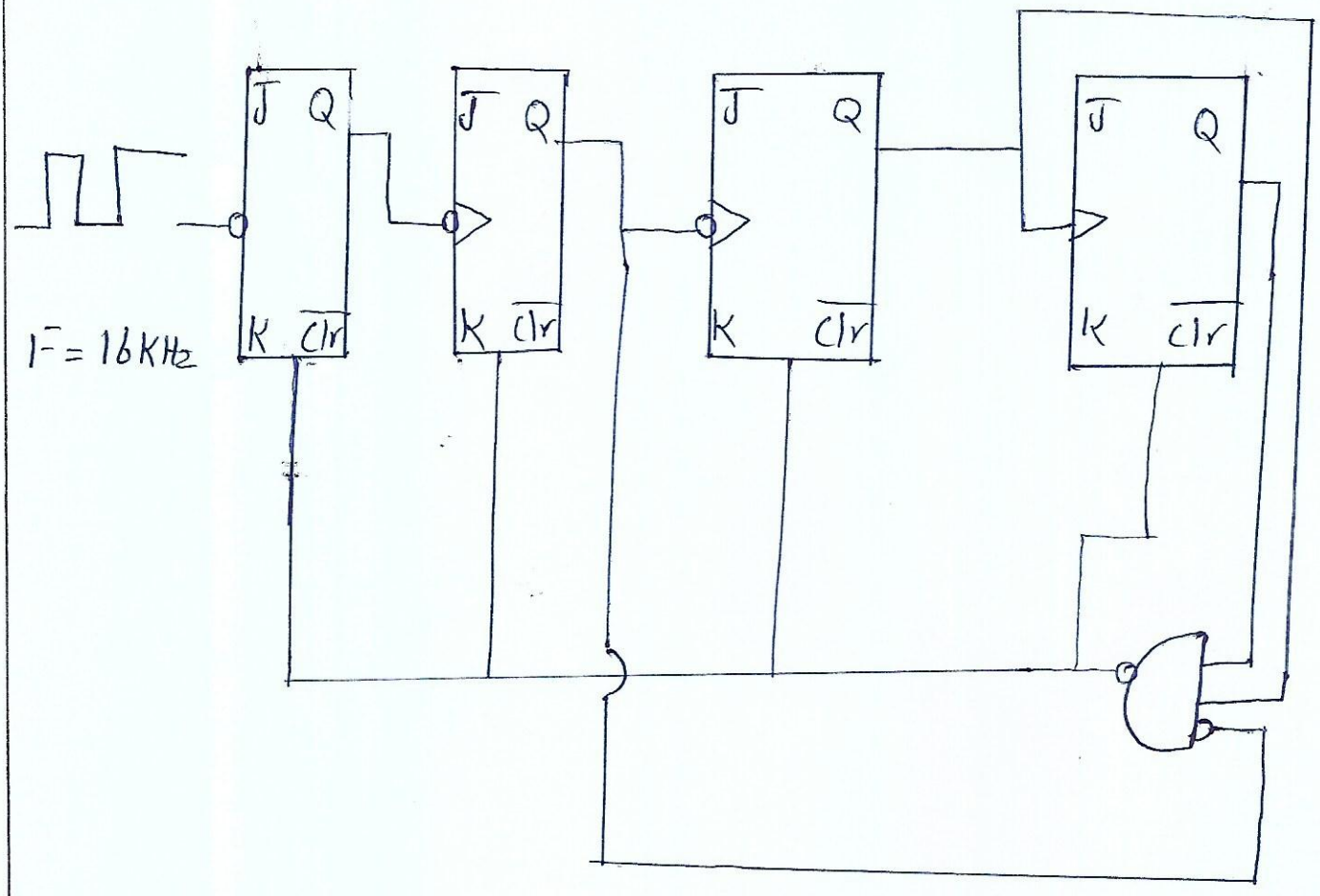
Input	output			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1





Q1 (D)

Frequency divider (use 3 J-K flip-flops and assume 16 KHz frequency of the initial wave-form.



(A) 0.833 KHz (B) 1.0 KHz

(C) 0.91 KHz (D) 0.77 KHz

Q2

Solution

Find the output [Y] if the select inputs are given.

a) $S_0 = 1, S1 = 0$

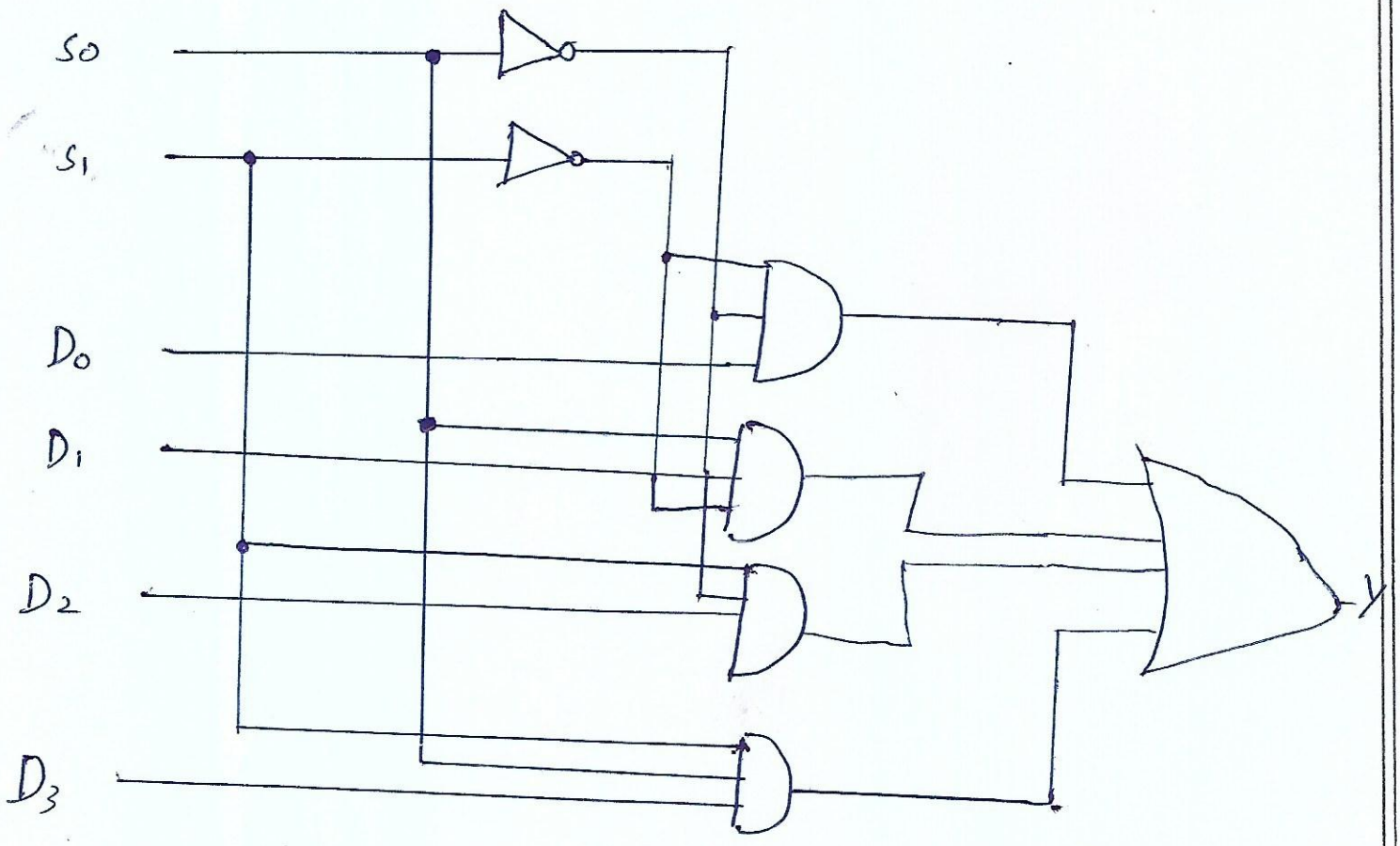
b) $S_0 = 0, S1 = 1$

c) $S_0 = 1, S1 = 1$

D) $S_0 = 0, S1 = 0$

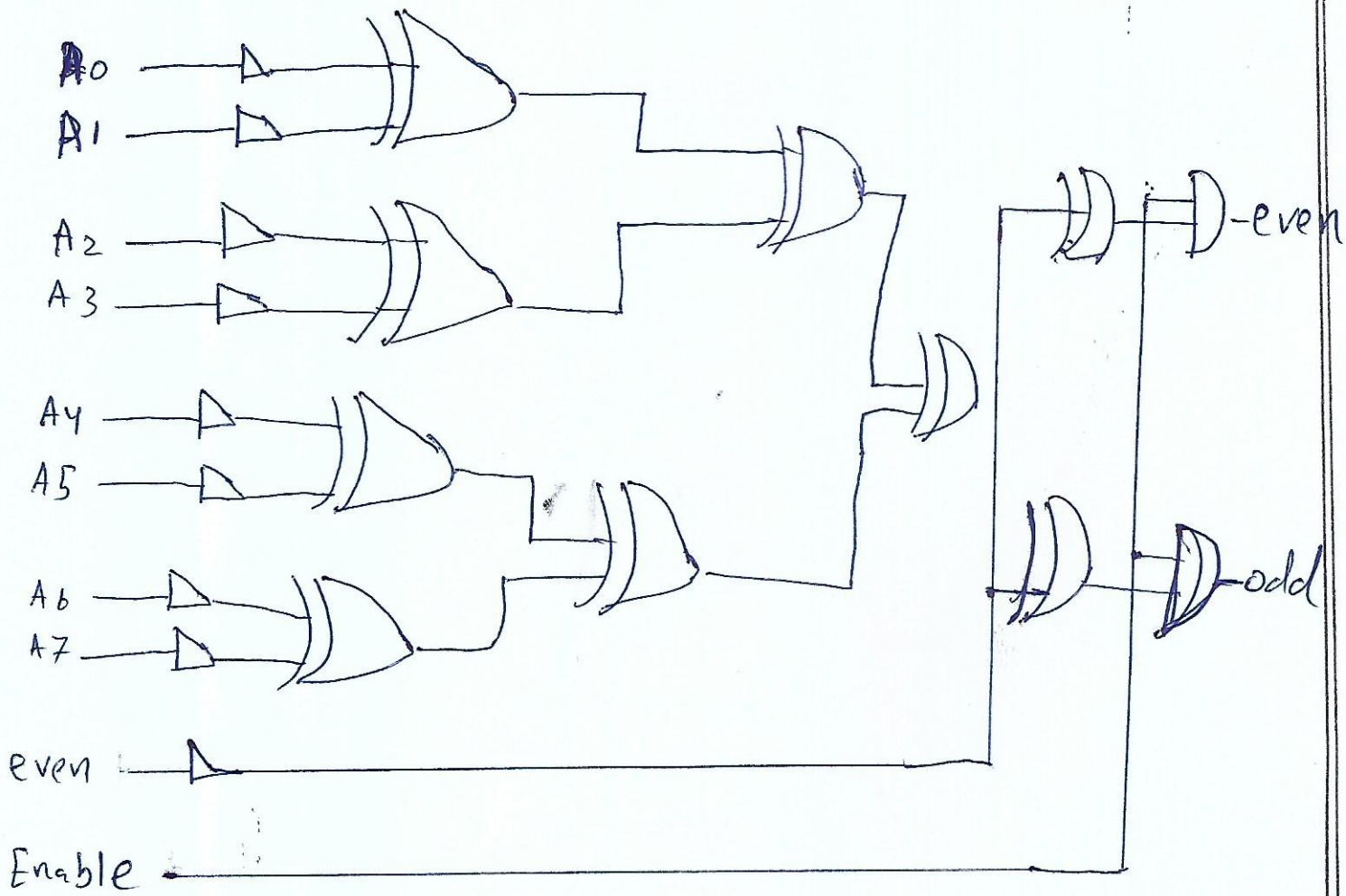
AS we know

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

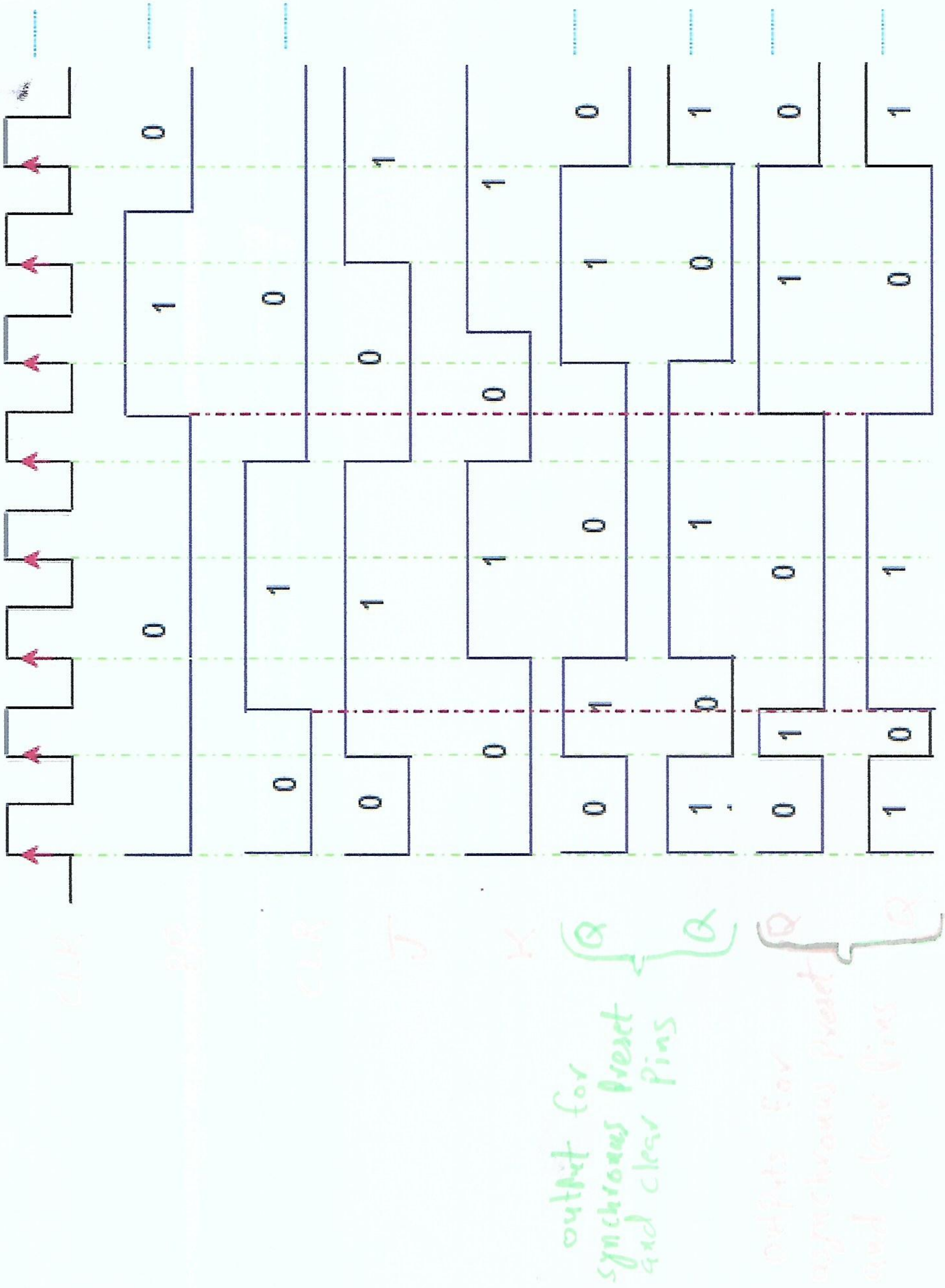


Q3 Timing diagram in Fig (01) shows inputs to a 9-bit Parity checker. Draw the Σ Even and Σ odd output for the even Parity checking.

Diagram

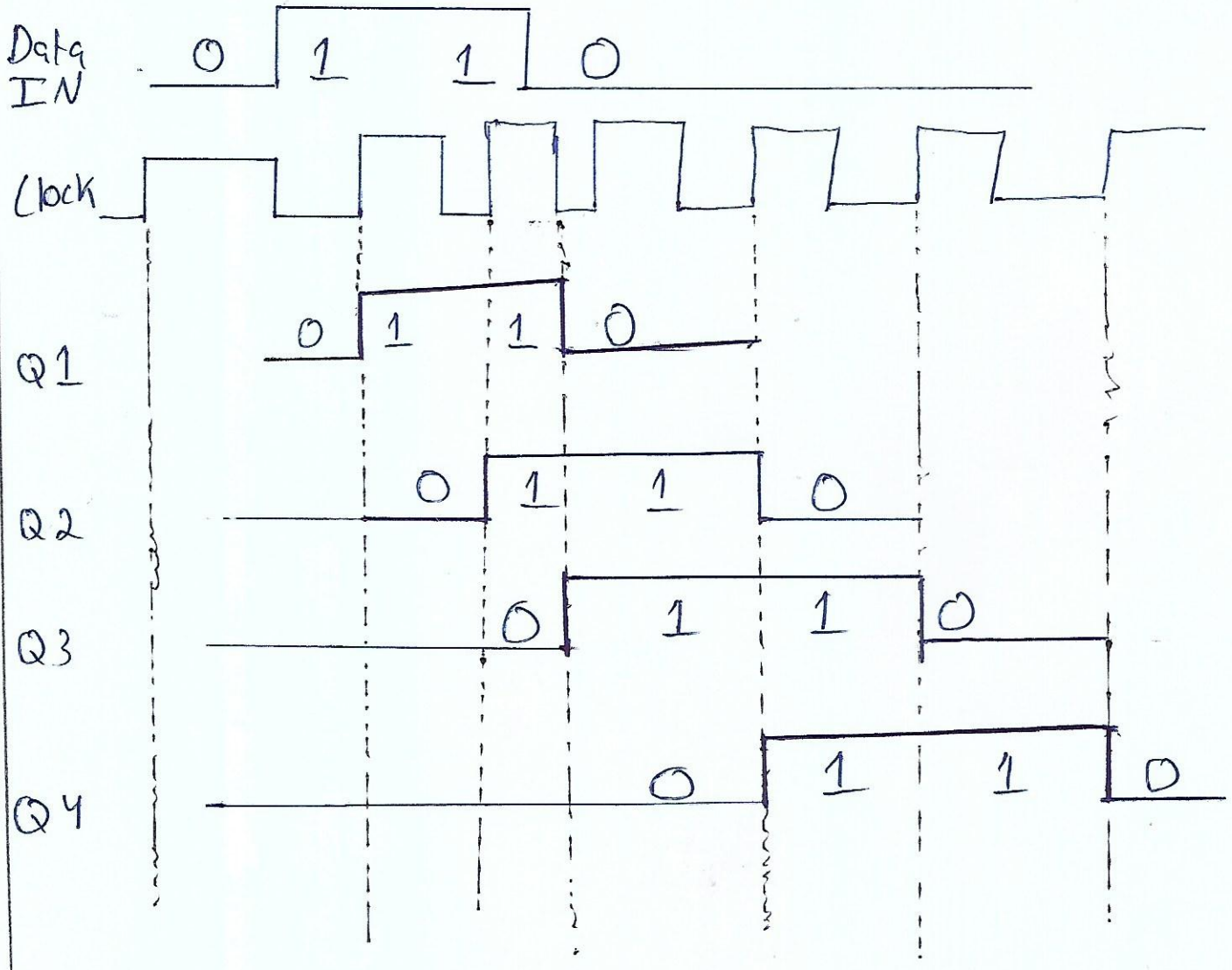


Q4

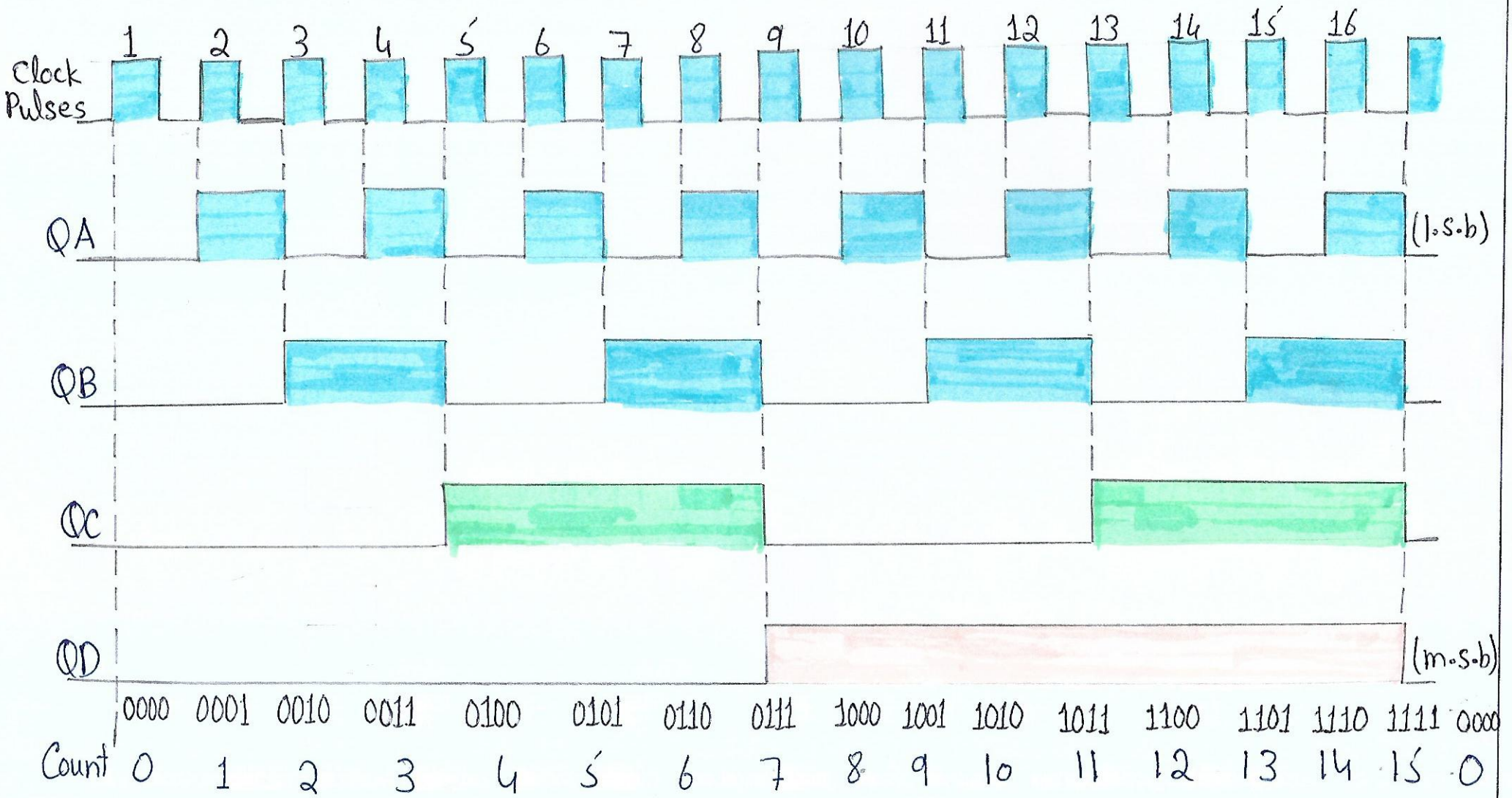


(Q.5) use the waveforms in Fig (03) to draw the timing diagram for the parallel outputs (Q1, Q2, Q3, Q4) For the shift register. Assume that register is initially cleared.

Diagram



Q 6


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
Clock Pulses
QA
(l.s.b)
QB
QC
QD
(m.s.b)
0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111 0000
Count 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0