Summer Final.

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Subject.	EDC- 1.

QNo1: The 1N4747 Zener diode used. The regulator current in figure Vs 20V

$V_Z = 20V \quad I_Z = 12.5mA$

$I_{ZK} = 0.25mA \quad Z_Z = 22\Omega$

a) for I_{ZK}

$V_{out} = V_Z - \Delta I_Z - I_Z$

$= 20V - (I_Z - I_{ZK})Z_Z$

$= 20V - (12.5mA - 0.25mA)22\Omega$

$= 20V - (12.25mA)22\Omega$

$= 20V - 0.269V$

$= 19.73V.$

$V_{out} = 19.73V.$

Calculate the zener diod maximum current. the power dissipation is 1w

$I_{Zm} = P_D(max) / V_Z = 1w / 20V = 50m$

for I_{Zm}.

$V_{out} = V_Z + \Delta I_Z Z_Z$

$= 20 + (I_{Zm} - I_Z) Z_Z$

$= 20V + (50mA - 12.5mA)22\Omega$

$= 20V + (37.5mA)(22)$

$V_{out} = 20V + 0.825$

$V_{out} = 20.825V.$

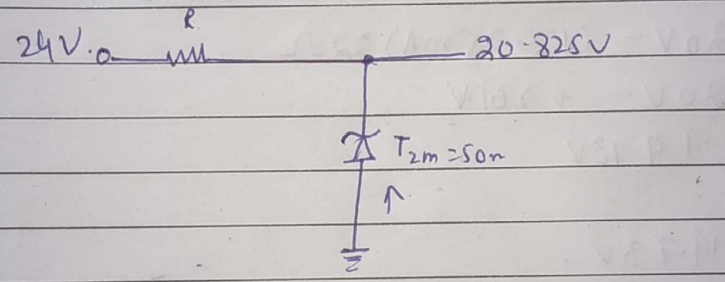
b) Calculate the value of R for zener current when there is no load as shown in figure.

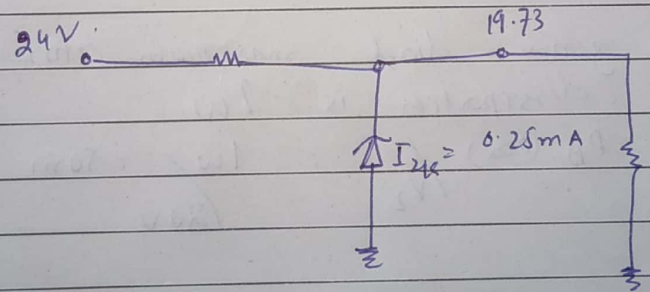
$$R = \frac{V_{IN} - V_{out}}{I_{zm}}$$

$$= \frac{24 - 20.825V}{50mA.}$$

$R = 63.5\Omega.$

$R = 70\Omega$ (Nearest largest standard).





for max load resistance (max current) the zener diode current minimum.

($I_{zk} = 0.25$)

$$I_1 = \frac{V_{IN} - V_{out}}{R} = \frac{24V - 19.73V}{70\Omega}$$

$I_1 = 0.061A.$

$= 0.061A.$

$I_T = 61mA.$

$I_L = I_T - I_{2K}.$

$= 61 - 0.25mA.$

$I_L = 60.75mA.$

$R_L = V_{out}/I_L = \frac{19.3}{60.75} = 19.3/60.75.$

$= 19.3/0.0675$

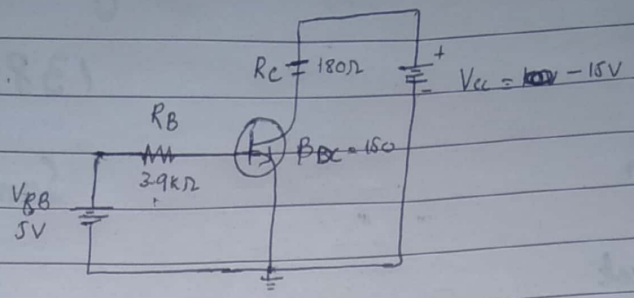
$= 285.92\Omega.$

$R_L = 286\Omega.$

Question NO 2.

Ans:

$V_{BE} = 0.7V$



Given data:

$V_{BB} = 5V$

$V_{cc} = -15V$.

$R_B = 3.9K\Omega$

$\beta_{DC} = 150$

$R_C = 180\Omega$

Required data:

I_B, I_C, V_{BE}, V_{CE}, V_{CB}.

Solution:

$$I_B = \frac{V_{RB} - V_{BE}}{R_B} = \frac{5V - 0.7V}{3.9K\Omega} = \boxed{1102\mu A}$$

$I_C = \beta_{DC} * I_B = (150)(1102\mu A) = \boxed{165.3mA}$

$= I_E = I_C + I_B = 165.mA + 1102\mu A = \boxed{166.4mA}$

Solve for V_{CE} & V_{CB}.

$V_{CE} = V_{cc} - I_C R_C = 15V(165.3mA)(180\Omega)$

$= 15V - 29.7V.$

$= \boxed{-14.7V}$

$V_{CB} = V_{CE} - V_{BE} \Rightarrow -14.7V - 0.7V.$

$= \boxed{-15.4V}$

Since the collector is at a lower voltage then the base, the collector-base junction is forward biased.

Question No 3.

Answer:

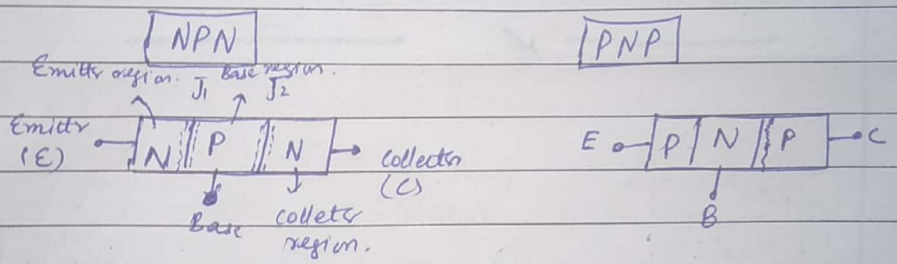
Bipolar Junction Transistors.

⇒ BJT:→

Transistor as:

* Invented in Dec 1947 at bell labs at USA
* BJT is a three terminal device and it is used in amplification of weak signals used in switching operation.

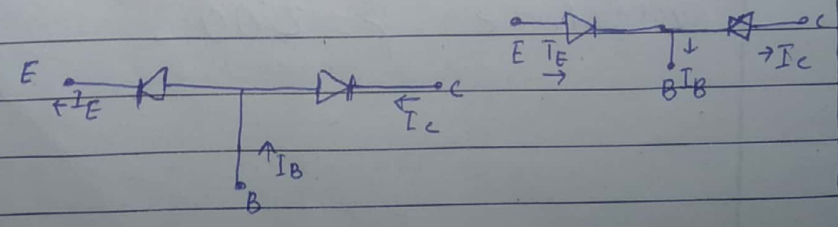
→ physical structure:



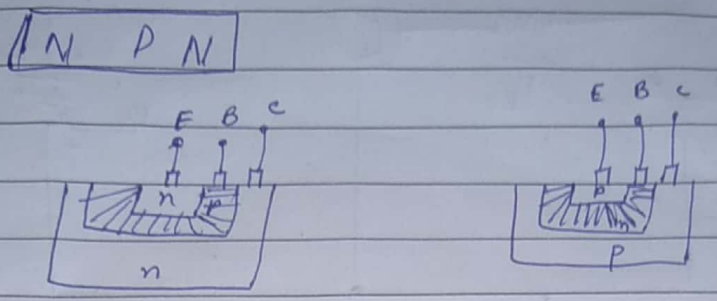
* 2 junction (N)
* 1 " (P)
* J_1 → emitter - base
* J_2 → collector - base
* There is depletion region at J_1
* There is depletion region at J_2.

width → E > B > C

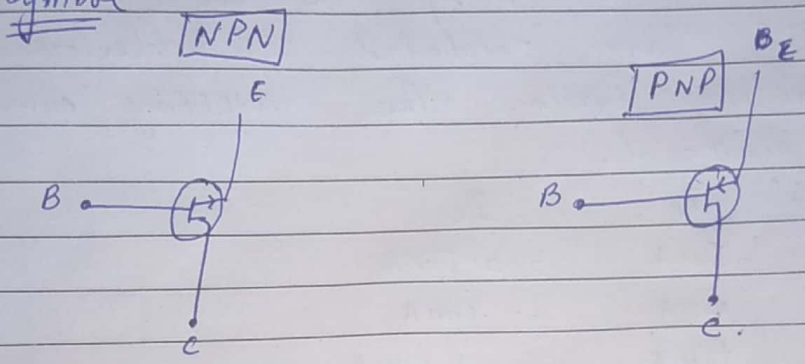
doping → E > B <> C



Cross Section view:



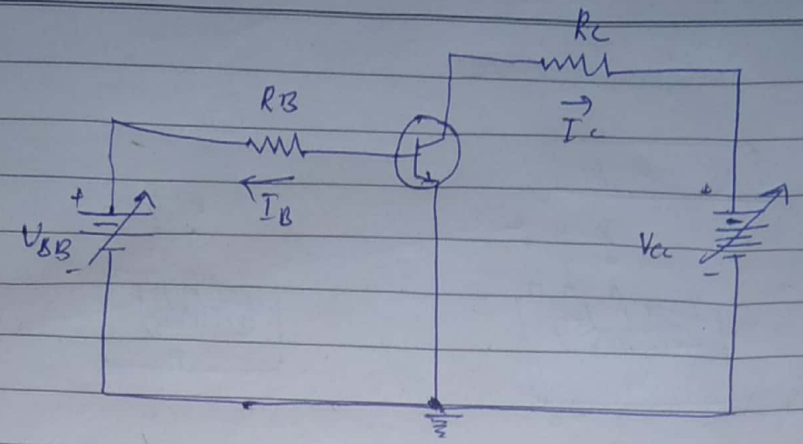
Symbol



- Increase of NPN the e will more from B → E.

Basic Configuration:

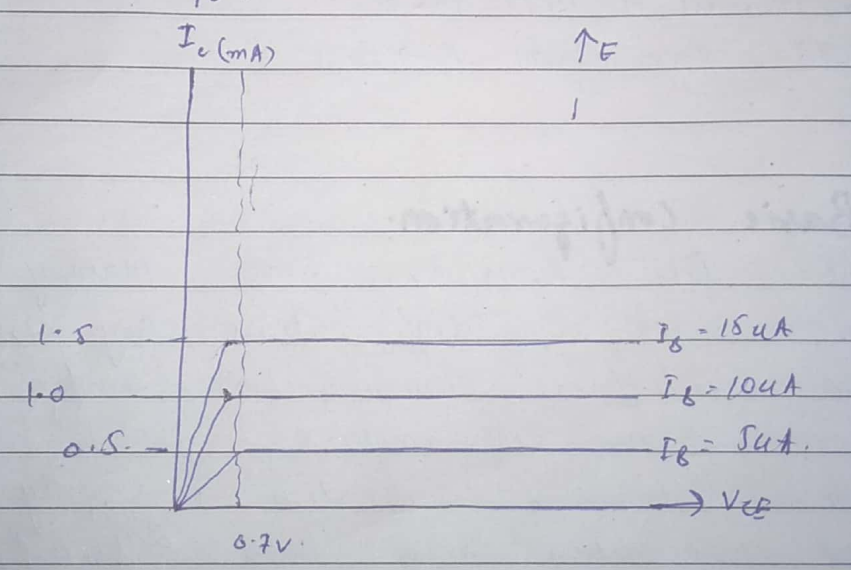
The BJT transistors have mainly three types of configurations. they are comm - emitters, common- base and comm - collector configuration.
common- emitter configratim is mostly used type. these three have different characteristics corresponding to both input and output signals. And also these three configuratem have few similarities.



using the relationship $I_C = \beta_{DC} I_B$ value of I_C are calculated and tabulated in below table. The resulting curves are plotted.

Table.

I_B	I_C
5uA	= 0.5mA
10uA	= 1mA
15uA	= 1.5mA



Question no 4.

Answer.

Transistor fully ON (ON)
Transistor fully OFF (OFF)
Input and base are at 0V (OFF)
Collector Current $I_c = 0$ (OFF)
$V_{CE} = V_{cc}$ (OFF)
BE junction is reverse base (OFF)
BC junction is forward base (OFF)
Max. of Saturation current I_c flows (ON)
BE junction is forward bias (ON)
$V_{CE} = 0V$ (ON)
BE function is less than 0.7V (OFF)

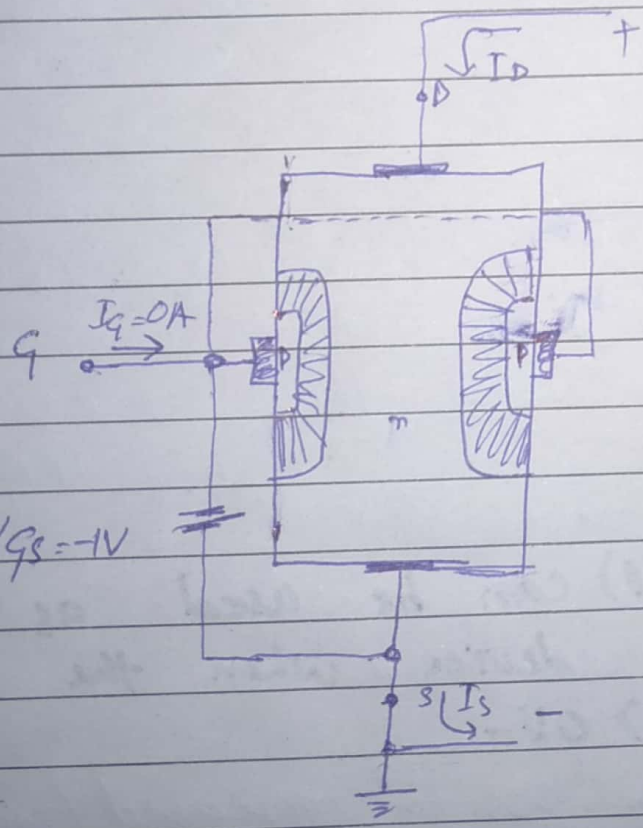
Question No 5.

Answer:

$V_{GS} < 0V$

V_{GS} is the voltage from gate to source and is the controlling voltage of the JFET.

For the n-channal device the controlling voltage V_{GS} is made more and more negative. From its $V_{GS} = 0V$ level. In other words, the gate terminal will be set at lower and lower potential levels as compared to the source.



In the figure, a negative voltage of -1V has been applied b/w the gate and source terminals for a low level of V_{DS}

The effect of the applied -ve-bias V_{GS} is to establish depletion region similar to those obtained with $V_{GS} = 0V$ but at lower level of V_{DS}.

The result of applying a negative bias to the gate is to reach the saturation level at a lower level of V_{DS}.

The resulting saturation level for I_D has been reduced and in fact will continue to decrease as V_{GS} is made more and more negative.

The pinch-off voltage continue to drop in parabolic manner as V_{GS} become more and more negative.

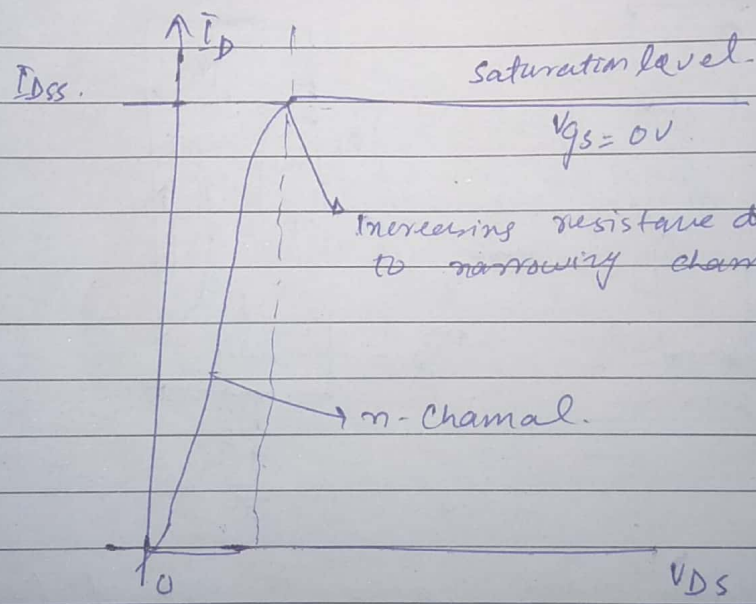
Eventually, V_{GS} when $V_{GS} = -V_p$ will be sufficiently negative to establish a saturation level that is essentially 0mA. for all practical purpose the device has been "turned off".

The level of V_{GS} that results in $I_D = 0mA$ is defined by $V_{GS} = V_p$ with V_p being a negative for - n-channal device and positive voltage for p-channal JFETs.

JFET (n-channal) can be used as voltage control device when the value of $V_{DS} > 0V$.

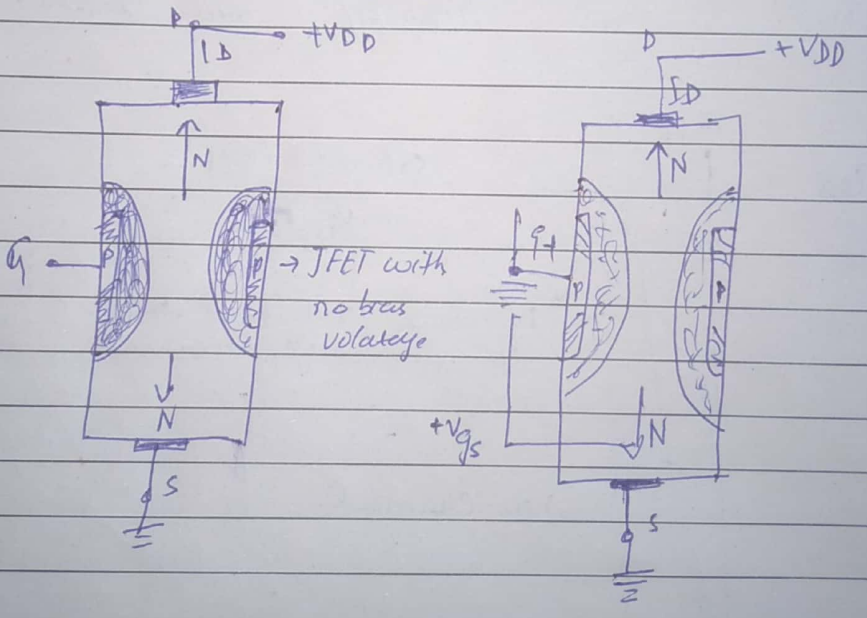
As the voltage V_{DS} is increased from 0 to a few volts the currents will increase as determined by Ohm's law.

The relative straightness of plot reveals that for the region of low value of V_{DS}, the resistance is essentially constant. As V_{DS} increase and approaches a level referred to as V_p, the depletion region will widen. Causing a noticeable reduction in the channal width. The reduced path of conduction causes the resistance to increase and the curve in the graph occure. The more horizontal the curve, the higher the resistance. If V_{DS} is increased to a level where it appears that the two depletion region would touch as shown in the figure. the conduction is referred to as "pinch off" will result.



In the Saturation region, the level of I_D remain essentially same. therefore once $V_{DS} > V_p$ the JFET has the characteristics of a source current.

Polarity Conventions: JFET The polarity for N-channal and P-channal JFET's are shown in fig. In bothe of the cases the voltage b/w the gate and Sources is such that the gate is reverse biased. This is normal method of connection of JFETs. The drain and Soarce terminal are interchangable, that is either end can be used as drain. The Soarce terminal is always connected to that end of the drain voltage supply whichrich provide the necessary chorges carries terminal S is connected to the nagative end of the drain voltage supply for obtaing



1.

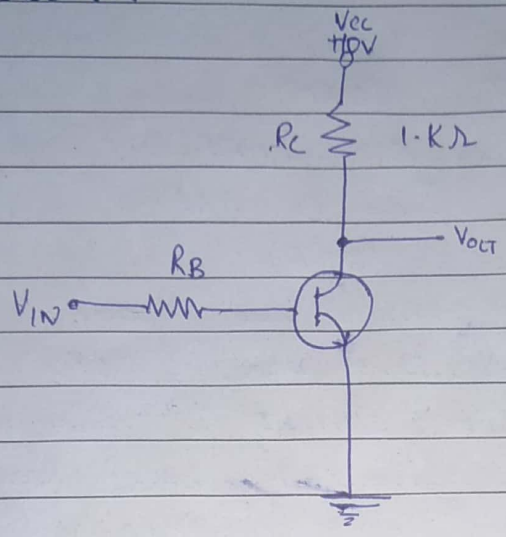
1. When neither any bias is applied to the gate (i.e when $V_{GS}=0$) nor any voltage to the drain w.r.t Source (i.e when $V_{DS}=0$) the depletion regions around P-N junctions are of equal thickness and Symmetrical.

2) when +ve voltage is applied to the drain terminal D w.r.t Source terminal S without connecting gate terminal G to supply. as shown. the electrons (majority carrier) flows from terminal S to terminal D. whearas conventional drain current D flow through the channal from D to S. Due to flow of this current there is uniform voltage drop across the channal resistance as we move from terminal D to terminal S. This voltage drop reverse biases the diod. The gate is more -ve withe respect to those points to D than to S. there depletion region layers pentrate more deeply into the channal. at points lying closer to D than to S. Thus wedge-shaped depletion region are formed.

To see how the width of the channal. varies with the variation in gate voltge. let us assume that the gate is -ve biased with respect to ~~current~~ Source while the drain is applied with +ve biase with respect to the source The P-N junction are then revese biased ande depletion regions are formed. P- region are heavily droped compared to the N- channal. So the depletion regions penetrate deeply into the channal. Sine a depletion region is a regions depleted of the charged carrier it behaves as an Insulator.

Question No 6.

Solution:



Given data:

$\beta_{DC} = 125$

$V_{CE(sat)} = 0.4V$

$V_{cc} = 10V$

$R_c = 1K\Omega$.

Required:

$V_{CE} = ?$ $I_B = ?$

Sol:

(a) @ $V_{CE} = ?$ $V_{IN} = ON$.

when $V_{IN} = ON$, So transistor is in cutt off mode and

$V_{CE} = V_{cc} = 10V$.

(b) min $I_B = ?$ $\beta_{DC} = 125$. $V_{CE} = 0.4$.

$$I_{c(sat)} = \frac{V_{cc}}{R_c} = \frac{10V}{1K\Omega} = 10mA.$$

$$I_{B(min)} = \frac{I_{c(sat)}}{B_{DC}} = \frac{10mA}{125} = \boxed{80\mu A}$$