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Semester: 4th

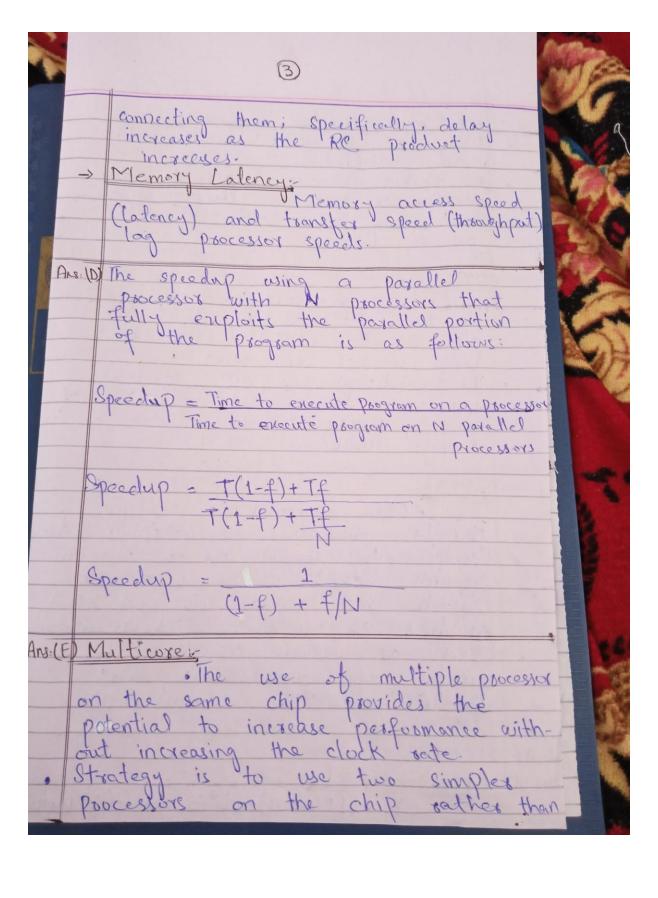
*ID* # : <u>15366</u>

Sessional Assignment No : 2nd

Subject : <u>Computer Architecture</u>

Submitted To: Muhammad Amin Sir

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7	9	
	one more complex processos.  Nith two processors larger caches  are justified.  As caches became larger it made  performance sense to create two  and then three levels of cache  on a chip.	
	MIC:  Leap in performance as well  as the challenges in developing  software to emploit such a  longe number of cores.  The multicose and MIC strategy  involves a homogeneous collection of  general purpose processors on a  single chip.	
	GPUs: Core designed to perform  parallel operations on graphics data.  Traditionally found on a plug-in  graphics card, it is used to  encode and render 2D and 3D  graphics as well as process video.  Used as vector processors for a  variety of applications that  require repetitive computations.	
G2 Ans (	Effective CPI:- (PT = (1*46000)+(2*33000) + (2*16000)	

(5) + (2\* 9000)/100 CPI = 162000/100 CPI = 1620 MIPS Rate: MIPS Rate = 60 M Hz / 1620 \* 106 MIPS rate = 60 x 106 Hz / 1620 \* 105 MIPS rate = 0.037 Execution Time: Ic/(MIPS \* 106) T = 104000/(0.037 \* 106) T = 2811 \* 10-3 T 2 2.811 Sec Ans: 18) For Machine A.  $CPI = (1*8 + 3*4 + 4*2 + 3*4) * 10^{6}$   $(8+4+2+4) * 10^{6}$ CPI = 40 CPI = 2.22

 $CPI = \frac{(1*10+2*8+4*2+3*4)*10^6}{(10+8+2+4)*10^6}$ 

CPI = 46/24

CPI = 1.92

MIPS rate = 200 MHz / 1.92 x 106

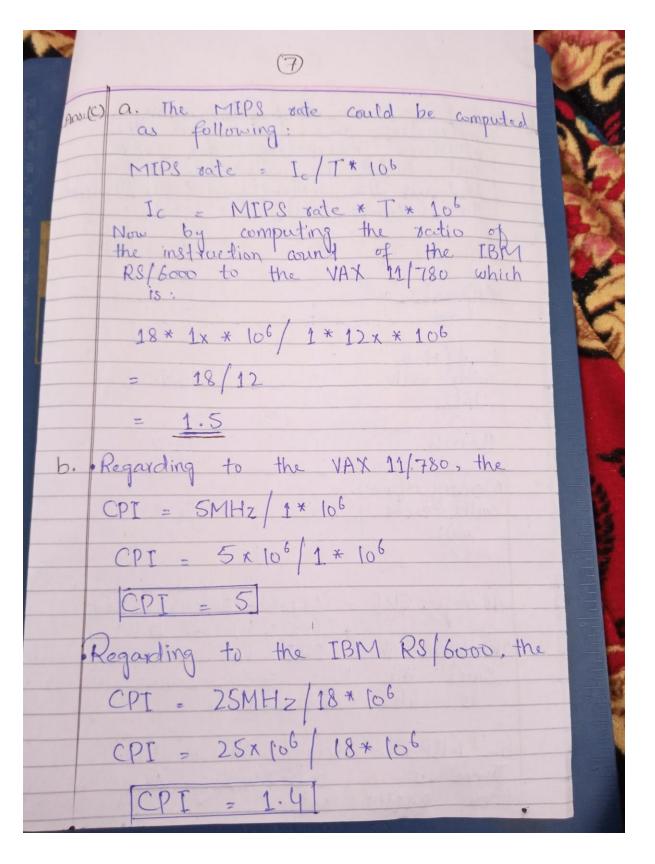
MIPS rate = 200 \* 106/1.92 \* 106

MIPS rate = 1041.

T = Ic (MIPS \* 106)

= 24 \* 10 \$ 104 \* 106

= 0.23 sec



And In Control	-(8)	H- same	
task could	mix, the	at means the  ns for each  llocated appropriately  ction types. Therefore,  be gotten:	THE RESERVE TO A SECOND
Instruction Type	Cbl	Instruction Mix	
Arithmetic and Logic	1	60.1.	STATE OF THE PARTY
Load / store with cache hit	2	18.1.	
Branch	4	12.(-	
Memory reference with cache miss	12	10 /,	
V	+ (1) x 0.	+(2x0.18) + (4x0.12) 1) = 2.64. has been inexessed	
Since the	time to	Bossa umman x	
b. MIPS = There is a the MIPS	400/2. corresponde.	64 = 152. anding deop in	

c. The speedup factor equals to the ratio of the execution times. The execution time is calculated as the following: Te/(MIPS \* 106) For one processor, T1 = 2 \* 106/178 \* 106 For the 8 processors, each processor executes 1/8 of the 2million instructions plus the 25,000  $T_8 = 2 \times 10^6 / 8 + 0.025 \times 10^6$ To = 1.8 ms Therefore we have Speedup = 11/1.8 Speedup = 6.11 do By deponding on the information given, it is not obvious how to quantity this effect in Amdahl's equation. Therefore, if it is supposed that the fraction of code, which is parallelizable, is f = 1, then Amdahl's law decreases to speedup = N = 8. Therefore, the actual speedup (10) the