IQRA NATIONAL UNIVERSITY
Phase II, Hayatabad peshawer

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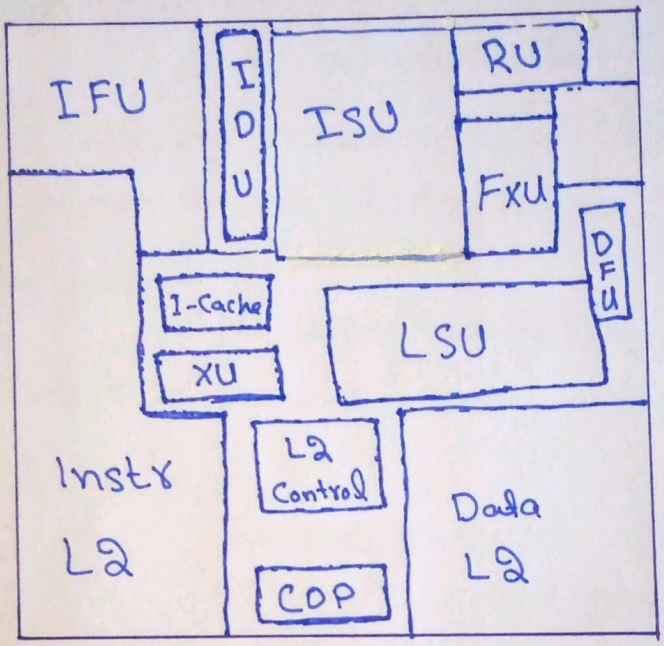
Dept: BS(CS) (1) paper: Computer Architecture

Q1:- Part(A)

Ans:-




Function of each Sub-area:-

⇒ Instruction Sequence unit (ISU):- Determine the Sequance in which instruction are executed in what is referred to as a Superscalar architecture.

⇒ Instruction fetch unit (IFU):- Logic for fetching instructions.

⇒ Instruction decode unit (IDU):- The (IDU) is fed from the IFU buffers and is responsible for the parsing and decoding of all Z/Architecture operation codes.

⇒ Load-Store unit (LSU):-
It is responsible for handling all types & operand accesses & all lengths, modes and formats as defined in the z/Architecture.

⇒ XU (translation unit):-
This unit translates logical address from instructions into physical address in main memory.

⇒ Fixed-point unit (FXU):-
The FXU executes fixed-point arithmetic operations.

⇒ Binary floating-point unit (BFU):-
The (BFU) handles all binary and hexadecimal floating-point operations as well as fixed-point multiplication operations.

⇒ Decimal floating-point unit (DFU):-
The DFU handles both fixed-point & floating-point operations on numbers that are stored as decimal digits.

⇒ Recovery unit (RU):-
The RU keeps a copy of the complete state of the system that includes all registers, collects hardware fault, signals etc.

⇒ Dedicated Co-processor (Cop) :-
The Cop is responsible for the data compression and encryption function for each core.

⇒ I-Cache :-
This is a 64-KB L1 instruction cache. allowing IFU to prefetch instructions before they are needed

⇒ L2 Control :-
This is a control logic that manages the traffic through the two L2 caches.

⇒ Data L2 :-
A 1-MB L2 data cache for all memory traffic others than instructions.

⇒ Instr-L2 :-
A- 1-MB L2 instruction Cache.

Ans - Part (B):-

IAS operation:-

The IAS operates by repetitively performing an instructions cycle. Each instruction cycle consiste of two sub-cycles.

① Fetch cycle:- During fetch cycle. the opcode of the next instruction is loaded into the IR and the address portion is loaded into the MAR. This instructions may be taken from the IBR. or it can be obtained from memory by loading a word into the MBR, and then down to the IBR, IR and MAR.

② Execute cycle:- Control circuity interpret the opcode and executes the instruction by sending out the appropriate control signals to cause data to be moved or an operation to be performed by the ALU.

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Ans – part (c) :-

Embedded System :-

The term embedded system refers to the use of electronics and Software within a product as opposed to a general purpose computer, such as a laptop or desktop system. Today, many devices that use electric power have an embedded computing system

Different embedded system used in everyday life are!

cell phones, digital cameras, video cameras, calculators microwave ovens, home security system, washing machine lighting system, printer etc.

Ans – part (D) :-

Different destop applications that require the great power of contemporary microprocessor based system

* Image processing
* Three-dimensional rendering
* Speech recognition
* Video conferencing
* Multimedia authoring
* voice and video annotation of files
* Simulation modeling

Ans-part (E):-

The technique used in contemporary processors to increase speed are following.

⇒ Pipelining:- Pipelining enables a processor to work simultaneously on multiple instructions by performing a different phase for each of the multiple instructions at the same time.

⇒ Branch prediction:- Branch prediction potentially increase the amount of work available for the processor to execute.

⇒ Superscalar Execution:- This is the ability to issue more than one instruction in every processor clock cycle. In effect, multiple parallel pipelines are used.

⇒ Data flow analysis:- The processor analyze which instructions are dependent on each other's result, or data, to create an optimized schedule of instructions

⇒ Speculative excution:- This enables the processor to keep its execution engines as busy as possible by executing instructions that are likely to be needed.

Ans-part (F) :-

The problems created due to increase in clock speed and logic density of the processor are;

Power :- As the density of logic and the clock speed on a chip increase. So does the power density the difficulty of dissipating the heat generated on high-density, high speed chips is becoming a serious design issue.

Rc delay :-

The speed at which electrons can flow on a chip between transistor is Limited by the resistance and capacitance of the metal wires connecting them, specifically. delay increases as the Rc product increases.

Memory Latency and throughput :-

Memory access speed (latency) and transfer speed (throughput) lag processor speeds.

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Ans – part (8) :-

Consider a program running on a single processor such that a fraction $(1-f)$ of the execution time involves code that is inherently sequential, and a fraction $f$ that involves codes that is infinitely parallelizable with no scheduling overhead. Let T be the total execution time of the program using a single processor. Then the speed up using a parallel processor with N processors that fully exploit the parallel portion of the program is as follows;

$$\text{Speedup} = \frac{\text{Time to execute program on a single processor}}{\text{Time to execute program on } N \text{ parallel processors}}$$

$$\text{Speedup} = \frac{T(1-f) + Tf}{T(1-f) + \frac{Tf}{N}} = \frac{1}{(1-f) + f/N}$$

Ans – part (H):- The use of multiple processors on the same chip, also referred to as multiple cores or multicore.

**Multicore:-**

Provides the potential to increase performance without increasing the clock rate.

- If the software can support the effective use of multiple processors then doubling the number of processors almost double performance.
- Two core chips were quickly followed by four-core chips, then 8, then 16, and so on.

**MIC :-**

The leap in performance as well as the challenges in developing software to exploit such a large number of cores has led to the introduction of a new term called many integrated core (MIC).

- The multicore and MIC strategy involves a homogenous collection of general-purpose processors on a single chip.

GPUs :- A GPU is a core designed to perform parallel operations on graphics data. It is found on a plug-in graphics card.

- It is used to encode and render 2D and 3D graphics as well as process video.
- GPUs perform parallel operation on multiple sets of data, they are increasingly being used as vector processors for a variety of applications that require repetitive computations.

Ans-part (I):-

QuickPath Interconnect (QPI) protocol Layer :-

- In this Layer, the packet is defined as the unit of tranfer
- The packet contents definition is standaradized with some flexibility allowed to meet differing market segment requirements.
- One key function performed at this layer is a cache coherency protocol, which deals with making sure that main memory values held in multiple caches are consistent.

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Ans - part (J) :-

Physical and logical Architecture & PCIe :-

⇒ Root complex :-

It is also called "chipset" or host bridge which connects the processor and memory subsystem to the PCI Express switch fabric. Comprising one or more PCIe and PCIe switch devices.

- The root complex acts as a buffering device to deal with difference in data rates between I/O controllers and memory and processors components.

PCIe links from the chipset may attach to the following. kinds of devices that implement PCIe:

Switch :- The switch manages multiple PCIe streams.

PCIe endpoint :- An I/O device or controller that implements PCIe. Such as a Gigabit ethernet switch, graphics, disk interface etc.

legacy endpoint :- Legacy endpoint @legacy is intended for existing designs that have been migrated to PCI Express, and it allows legacy behaviors. Such as use of I/O space and Locked transactions.

PCIe/PCI bridge :- Allows older PCI devices to be connected to the PCIe-based systems.

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Q2 - part (A) :-

Ans:- Structural Components of Computer:-
There are four main structure components of computer

(1) Central processing unit (CPU):- It controls the operation of the computer and performs its data processing functions: often simply referred to as "processor"

(2) Main memory:- It can stores data

(3) I/O :- It moves data between the computer and its external environment.

(4) System Interconnecting:- Some mechanism that provides for communication among CPU, main memory and I/O. A common example of system interconnection is by means of a "system bus".

Ans - part (B) :- The characteristics of computer family are as follows:

Similar or identical instruction set:-
In some cases, the lower end of the family has an instruction set that is a subset of that of the top end of the family. This means that programs can move up but not down.

Similar or identical operating system:-
The same basic operating system is avaible for all family members.

Increasing speed:- The rate of instruction execution increases in going from lower to higher family members.

Increasing number of I/O ports:-
The number of I/O ports increases in going from lower to higher family members.

increasing memory size:-
The size of main memory increases in going from Lower to higher family members.

Increasing Cost:-
At a given point in time, the cost of a system increases in going from Lower to higher family members.

Ans - Part (C):-

Stored program Computer:-
A fundamental design approach first implemented in the IAS Computer is known as the "Stored-program Concept". This idea is usally attributed to the mathematician John von Neuman.

The first publication of the idea was in a 1945 proposal by von Neuman. for a new computer the EDVAC (Electronic Discrete Variable Computer) in 1946, von Neuman and his colleagues began the design of a new stored-program computer. ~~and~~ referred to as the IAS computer at the Princeton Institute for Advanced Studies, It Consist of;

→ A main memory, which stores both data and instructions.

→ An arithmetic and logic unit (ALU) capable of operating on binary data.

Ans – part (D) :-

Moore's Law :- The famous Moore's Law which was proposed by Gorden Moore, Co-founder of Intel, in 1965. Moore observed that the number of transistors that could be put on a single chip was doubling every year, and correctly predicted that this pace would continue into the near future. The consequences of Moore's Law are:

1) The cost of computer logic and memory circuitry has fallen at a dramatic rate.
2) The computer becomes smaller, making it more convenient to place in a variety of environments.
3) There is a reduction in power requirements.
4) The interconnections on the integrated circuit are much more reliable than solder connections.

Ans-part (E):-

Instruction Cycle State diagram:- The states in instruction cycle state diagram are follows:,

⇒ Instruction address calculation (iac):- Determine the address of the next instructions to be executed. Usually this involes adding a fixed number to the address of the previous instruction.

⇒ Instruction fetch (if):- Read instruction from its memory location into the processor.

⇒ Instruction operation decoding (iod):- Analyze instruction to determine type of operation to be performed and operand (s) to be used.

⇒ operand address calculation (oac):- if the operation involes reference to an operand in memory or available via I/O, then determine the address of the operand.

⇒ Operand fetch (of):- fetch the operand from memory or read it in form I/O.

⇒ Data operand (do):- perform the operation indicated in the instruction.

⇒ Operand Store (os):- write the result into memory or out to I/O.

Ans – part (F):- Classes of Interrupts

⇒ Program :- It is generated by some condition that occurs as a result of an instruction execution such as arithmetic overflow, division by zero attempt to execute an illegal machine instruction, or reference outside a users allowed memory space.

⇒ I/O :- It is generated by an I/O controller to signal normal completion of an operation request service from the processor, or to signal a variety of error conditions.

⇒ Timer :- It is generated by a timer within the processor. This allows the operating system to perform certain functions on a regular basis.

⇒ Hardware Failure :- It is generated by a failure such as power failure (or) memory parity error.

Ans - part (G) :-

Bus Interconnection Scheme :- The most common computer interconnection structure are based on the use of one or more system buses.

A system bus consiste typically of about fifty to hundreds of separate lines. The lines can be classified. into three functional groups; data address and control Lines.

⇒ Data lines :-

The data lines provide a path for moving data among system modules. These lines, collectively are called the "data bus". The data bus may Consiste of 32, 64, 128 or greater separate lines.

⇒ Address lines :-

The address lines are used to designate the source on the data bus. The width of the address bus determines the maximum possible memory capacity of the system.

⇒ Control Lines :- The control lines are used to control the access to and the use of the data and address lines, Because the data and address lines are shared by all components.

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Q3- part (A):-

Ans:-

| Computer orgnization | Computer Acchiteeture |
|---|---|
| • Computer orgnization refers to the operational units. and their interconneetions that realize the architeeture specifications. | • Computer architeeture refers to those attributes put another that have direct impact on the logical execution & a program<br>• A term that is often used interchangeably with computer architeeture is "instruction set architeeture. |

part (B):-

CISC:- The current x86 offering represents the result & decades & design effort on "Complex instruction set computers" (CISC).

The x86 incorporates the sophisticated design principles once found only on main frames and super-computer and serves as an excellent example & CISC.

RISC:- An alternative approach to processor design is the "reduced instruction set computer (RISC).

The ARM architeeture is used in a wide variety & embedded system and is one & the most powerful and best-designed RISC-based systems on the market.

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Ans - part (c) :-

**Microprocessor :-** A microprocessor chips included register an ALU, & some sort of control unit or instruction processing Logic. As transistor density increased. It became possible to increse the complexity of the instruction set architecture and ultimately to add memory and more than one processor. Microprocessor includes multiple core and little amount of cache memory.

**microcontroller :-** A microcontroller is a single chip that contains the processor non-volatile memory for the program (ROM), volatile memory for input and output (RAM), a clock and an I/O control unit. The processor portion of the microcontroller has a much lower silicon area than other microprocessors and much higher energy efficiency.

Ans - part (D) :-

**Cortex - A :-** The Cortex-A and Cortex-A50 are application processors. intended for mobile devices such as Smart Phones and ebooks readers, as well as consumer devices such as digital Tv and home gateways.

**Cortex-R :-** The Cortex-R is designed to support real-time applications, in which the timing of events needs to be controlled with rapid response to events. They have run at a fairly high clock frequency and have very Low respone latiency.

**Cortex-M :-** Cortex-M series processor have been developed primarily for the microcontroler domain where the need for fast highly deterministic interrupt management is coupled with the desire for extremely Low gate count and Lowest possible power consumption.

Ans-part(E):-

- In the interrupt cycle the processor checks to see if any interrupt have occured indicated by the presence of an interrupt signal
- if no interrupts are pending, the processor proceeds to the fetch cycle and fetches the next instruction of the current program.

Ans-part(F):-

Disabled Interrupt:- A disabled interrupt simply means that the processor can and will ignore that interrupt request signal. If an interrupt occurs during this time. It generally remains pending and will be checked by the processor after the processor has enabled interrupts. when user program is excuting and an interrupt occurs interrupts are disabled immediately.

Nested Interrupt :- nested interrupt is to allow interrupt of higher priority to cause a Lower-priority interrupt handler to be itself interrupted. A user program begins at t=0. At t=10 a printer interrupt occurs. User information is placed on the system stack and execution continues at the printer.

Ans – part (G) :-

Programing in Hardware :- The program is in the form of hardware and is termed as "hardware program" Suppose we construct a general purpose configuration of arithmetic and logic functions. This set of hardware will perform various functions on data depending on control signal applied to the hardware.

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Programming in Software :-

The new method & codes or instructions is called Software programming

In this method. programming is much easier. Instead & rewiring the hardware for each new program. all we need to do is provide a new sequence & codes. Each codes is in effect an instruction and part & the hardware interprats each instruction and generates control signals.

Q4 - part (A)

Ans The simple way to understand this problem. Give instruction are divided into two 5bit instruction, LH and RH.

LH instruction = 010FA
opcode = 01
address = 0FA

RH instruction = 210FB
opcode = 21
address = 0FB

Since this in hexadecimal form, you have to convert this number to binary form.

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**LH instruction:-**

01 = 00000001 = LOAD M(x)

M(x) refers to the memory address Location 0FA

The first 5bits & 08A should read-LOAD M(0FA)

**RH instruction:-**

21 = 00100001 = STOR M(x)

M(x) refers to the memory address Location 0FB

The second 5bits & 08A should read - STOR M(0FB)

Finally the assembly language code for 08A 010FA210FB is

LOAD M(0FA)
STOR M(0FB)

(2) given are divided up into two 5bit instruction LH and RH

LH instruction = 010FA
opcode = 01
address = 0FA

RH instruction = 0F08D
op code = 0F
address = 08D

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Convert a number into binary form

LH instruction:-

01 = 00000001 = LOAD M(x)

M(x) refers to memory address Location 0FA

The first 8bits & 08B should read- LOAD M(0FA)

RH instruction:-

0F = 00001111 = Jump + M(x, 0:19)

refers to memory address location 08D

The second 8bits & 08B should read- Jump + M(08D 0:19)

at last the assembly language code for 08B 010FA0F08D is;

LOAD M(0FA)

Jump + M(08D, 0:19)

(3) Content are divided upto two 8bits instruction,

LH instruction = 080FA

opcode = 02

address = 0FA

RH instruction = 210FB

opcode = 21

address = 0FB

This lages hexadecimal form, to convert the number to binary form.

LH instruction :-

02 = 00000010 = LOAD - M(x)

M(x) refers to the memory address Location 0FA

The first 8bits of 08C should read - LOAD - M(0FA)

RH instruction :-

21 = 00100001 = STOR M(x)

M(x) refers to the memory address Location 0FB

The second 8bits of 08C should read - STOR M(0FB)

Assembly language code for 08C 020FA210FB is LOAD - M(0FA)

STOR - M(0FB)

(b) (1) In 08A address, the M(0FA) transfer to the accumulator and transfer content of accumulator to memory Location 0FB.

(2) In 08B address, The M(0FB) transfer to the accumulator and take next instruction from Left half of M(080).

(3) In 08C address, the -M(0FA) transfer to the accumulator and transfer Content of accumulator to memory Location 0FB.

Ans (c):- Effective CPI :-

$$CPI = (1 * 46000) + (2 * 33000) + (2 * 16000) + (2 * 9000) / 100$$

$$CPI = 162000 / 100$$

$$CPI = 1620$$

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## MIPS Rate:-

$$\text{mips rate} = 60\ Hz / 1620 \times 10^6$$

$$\text{MIPS rate} = 60 \times 10^6 / 1620 \times 10^6$$

$$= 60\ Hz / 1620$$

$$= 0.037$$

## Execution Time:-

$$T = Ic / (MIPS * 10^6)$$

$$T = 104000 / (0.037 \times 10^6)$$

$$T = 104000 / 37 \times 10^3$$

$$T = 2811 \times 10^{-3}$$

$$T = 2.811\ Sec$$

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Ans.-(D):-

(a) Since we have same instruction mix. that means the additional instruction for each task could be allocated appropriately between the instruction types. Therefore, the following table be got.

| Instruction type | CPI | Instruction mix |
|---|---|---|
| Arithmetic and logic | 1 | 60% |
| Load/Store with cache hit | 2 | 18% |
| Branch | 4 | 12% |
| memory references with cache miss | 12 | 10% |

The average CPI $= (1 \times 0.6) + (2 \times 0.18) + (4 \times 0.12) + (12 \times 0.1)$

$\Rightarrow CPI = 2.64$

Therefore, The CPI has been increased since the time for memory access is also increased.

(b) MIPS = 400 / 2.64 = 152

There is a corresponding drop in the MIPS rate.

(c) The speedup factor equals to the ratio of the execution times.

The execution time is calculated as the following

$$I = I_c / (MIPS \times 10^6)$$

For one processor, $T_1 = (2 * 10^6) / (178 * 10^6)$

$$\boxed{T_1 = 11 \text{ ms}}$$

For 8 processor, each processor executes 1/8 of the 2million instructions plus the 25,000

$$T_8 = \frac{2 * 10^6 / 8 + 0.025}{152 \times 10^6}$$

$$\boxed{T_8 = 1.8 \text{ ms}}$$

$$\text{Speed up} = \frac{\text{Time to excute Program on a single processor}}{\text{Time to excute program on N: Parallel processor}}$$

speedup = 11 / 1.8

$$\boxed{\text{Speedup} = 6.11}$$

(d) By depending on the information given, it is not obvious how to quarlify this effect in Amdahl's Equation. Therefore if it is supposed that the fraction of code, which is parallelizable, is $f = 1$ then Amadahl's Law decreas to speedup $N = 8$. Therefore The actual speedup is only about 75% of the theoritical speedup.

Ans - Part (E):-

Six Steps:-

(1) ⇒ The PC contains 300, The address of ~~the~~ first instruction This value is loaded into the MAR.

⇒ The value in Location 300 (which is the instruction with the value 1940 in hexadecimal) is Loaded into the MBR. and the PC is incremented. These two steps can be done in parallel.

⇒ The value in the MBR is Loaded into the IR

(2) ⇒ The address portion of the IR (940) is Loaded into the MAR.

⇒ The value in Location 940 is Loaded into the MBR.

⇒ The value in the MBR is loaded into the AC.

(3) ⇒ The value in the PC(301) is loaded into the MAR.

⇒ The value in Location 301 (which is the instruction with the value 9941) is loaded into the MBR and the PC is incremented.

⇒ The value in the MBR is loaded into the IR

(4) ⇒ The address portion of the IR (941) is loaded into the MAR.

⇒ The value in location 941 is Loaded into the MBR

⇒ The old value of the AC and the value of Locations MBR are added and the result is stored in the AC.

(5) ⇒ The value in the PC(302) is Loaded into the MAR.

⇒ The value in Location 302 (which is the instruction with the value 2941) is Loaded into the MBR, and the PC is incremented.

⇒ The value in the MBR is Loaded into the IR.

(6) ⇒ The address portion of the IR (941) is Loaded into the MAR.

⇒ The value in the AC is Loaded into the MBR

⇒ The value in the MBR is Stored in Location 941.

Ans - part (F):-

(a) $2^{24}$ = 16 MBytes

(b) ⇒ if the local address bus is 32 bits, the whole address can be transferred at once and decoded in memory. However, because the data bus is only 16 bits, it will require 2 cycles to fetch a 32-bit instruction or operand.

⇒ The 16 bits of the address placed on the address bus can't access the whole memory.

(c) The program counter must be at least 24 bits Typically, a 32-bit microprocessor will have a 32-bits external address bus and a 32-bit program Counter, unless an chip segment registers are used that may work with smaller program counter. if the instruction register is to contain the whole instruction. It will have to be 32-bit long. If It will contain only the op code (called op code register then it will have to be 8 bits long.

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Ans- part (a):-

A bus cycle takes 0.25 MS, so a memory cycle takes 1 MS. If both operands are even aligned. It takes 2 MS to fetch the two operands if one is odd aligned. the time required is 3 MS. If both are odd aligned, the time required is 4 MS.