

Assignment #2

Name: Ikramullah
ID#: 15072
Department: BS(CS)

Ans#1

Different desktop application that require the great power of contemporary microprocessor based system

- ① image processing
- ② Three-dimensional rendering
- ③ speech recognition
- ④ video conferencing
- ⑤ Multimedia authoring
- ⑥ voice and video annotation of files
- ⑦ simulation and modelling.

Ans#2

Pipelining

Pipelining enables a processor to increase work simultaneously on multiple instructions by performing a diff phase for each of the multiple instructions at the same time.

Branch Prediction

Branch prediction potentially increase the amount of work available for the processor to execute.

Superscalar execution

This is the ability to issue more than one instruction are dependent on each other's

Data Flow Analysis

The processor analyzes which instructions are dependent on each other's, or data, to create an optimized schedule of instructions.

Speculative execution

This is the ability to issue the processor to keep its execution engines as busy as possible by executing instructions that are likely to be needed.

Ans#3

Multicore

The use of multiple processors on the same chip provides the potential to increase performance without increasing the clock rate.

Strategy is to use two simpler processors on the chip rather than one more complex processor.

With two processors larger caches are

MIC

Lead in performance as well as the challenges in developing software to exploit such a large number of cores.

GPUs

Core designed to perform parallel operations on graphics data.

Traditionally found on a plug-in graphic card.

used as vector processors for a variety of application that require.

Ans#4

Effective CPI

$$CPI = (1 * 46000) + (2 * 33000) + (2 * 16000) + (2 * 9000) / 100$$

$$CPI = 162000 / 100$$

$$CPI = 1620$$

Mips Rate

$$\text{Mips Rate} = 60 \text{ MHz} / 1620 * 10^6$$

$$\text{Mips Rate} = 60 * 10^6 / 1620 * 10^6$$

$$\text{Mips Rate} = 60 / 1620$$

$$\text{Mips Rate} = 0.037$$

Execution Time

$$T = I_c / (\text{Mips} * 10^6)$$

$$T = 104000 / (0.037 * 10^6)$$

$$T = 104000 / 37 * 10^3$$

$$T = 2811 * 10^{-3}$$

$$T = 2.811 \text{ sec}$$

Ans# 5

For Machine A

$$CPI = (1 \times 8 + 3 \times 4 + 4 \times 2 + 3 \times 4) \times 10^6 / (8 + 4 + 2 + 4) \times 10^6$$

$$CPI = 46 \times 10^6 / 18 \times 10^6$$

$$CPI = 2.22$$

$$\text{MIPS rate} = 200 \text{ MHz} / 2.22 \times 10^6$$

$$\text{MIPS rate} = 200 \times 10^6 / 2.22 \times 10^6$$

$$\text{MIPS rate} = 90.09$$

$$T = 10^6 / (\text{MIPS} \times 10^6)$$

$$T = 18 \times 10^6 / 90 \times 10^6$$

$$T = 0.2 \text{ sec}$$

For Machine B

$$CPI = (1 \times 10 + 2 \times 8 + 4 \times 2 + 3 \times 4) \times 10^6 / (10 + 8 + 2 + 4) \times 10^6$$

$$CPI = 46 / 24$$

$$CPI = 1.92$$

$$\text{MIPS rate} = 200 \text{ MHz} / 1.92 \times 10^6$$

$$\text{MIPS rate} = 200 \times 10^6 / 1.92 \times 10^6$$

$$\text{MIPS rate} = 104$$

$$T = 10^6 / (\text{MIPS} \times 10^6)$$

$$T = 24 \times 10^6 / 104 \times 10^6$$

$$T = 0.23 \text{ sec}$$

Ans#6

The MIPS rate could be computed as the following

$$\text{MIPS rate} = IC / T * 10^6$$

$$IC = \text{MIPS rate} * T * 10^6$$

$$18 * 1x * 10^6 / 1 * 12x * 10^6$$

$$= 18 / 12$$

$$= 1.5$$

Ans#7

Regarding to the VAX11/780 the CPI =

$$(25 \text{ MHz}) / (18 * 10^6) = 5 * 10^6 / 1 * 10^6$$

$$= 5 / 1 = 5$$

Regarding to the IBMRS/6000 the

$$\text{CPI} = (25 \text{ MHz}) / (18 * 10^6) = 25 * 10^6 / 18 * 10^6$$

$$= 25 / 18 = 1.4$$

Ans#8

Since we have the same instruction mix that means the additional instruction for each task could be allocated appropriately between the instruction types

Instruction Type	CPI	Instruction Mix
ALU	1	60%
Load/store with Cache Rt	2	18%

Branch	4	12%
Memory reference with cache miss	12	10%

$$\text{The average CPI} = (1 \times 0.6) + (2 \times 0.18) + (4 \times 0.12) + (12 \times 0.1) = 2.64$$

$$\text{MIPS} = 400 / 2.64 = 152$$

The speedup factor equals to the ratio of the execution times. The execution time is calculated as

$$T = IC / (\text{MIPS} \times 10^6)$$

$$\text{For the one processor, } T_1 = (2 \times 10^6) / (178 \times 10^6) = 11 \text{ms}$$

For the 8 processors, each processor executes $1/8$ of the 2 million instruction plus the 25000

$$T_8 = 2 \times 10^6 / 8 + 0.025 \times 10^6 / 152 \times 10^6$$

$$T_8 = 1.8 \text{ms}$$

Speedup = Time to execute program on a single processor / Time to execute program on N parallel processor

$$\text{Speedup} = 11 / 1.8$$

$$\text{Speedup} = 6.1$$

It is not obvious how to quantify this effect in Amdahl's equation. If it supposed that the fraction of code

which is parallelizable is $F=1$ then Amdahl's Law decreases to speedup = $N=8$. Therefore, the actual speedup is only about 75% of the theoretical speedup.