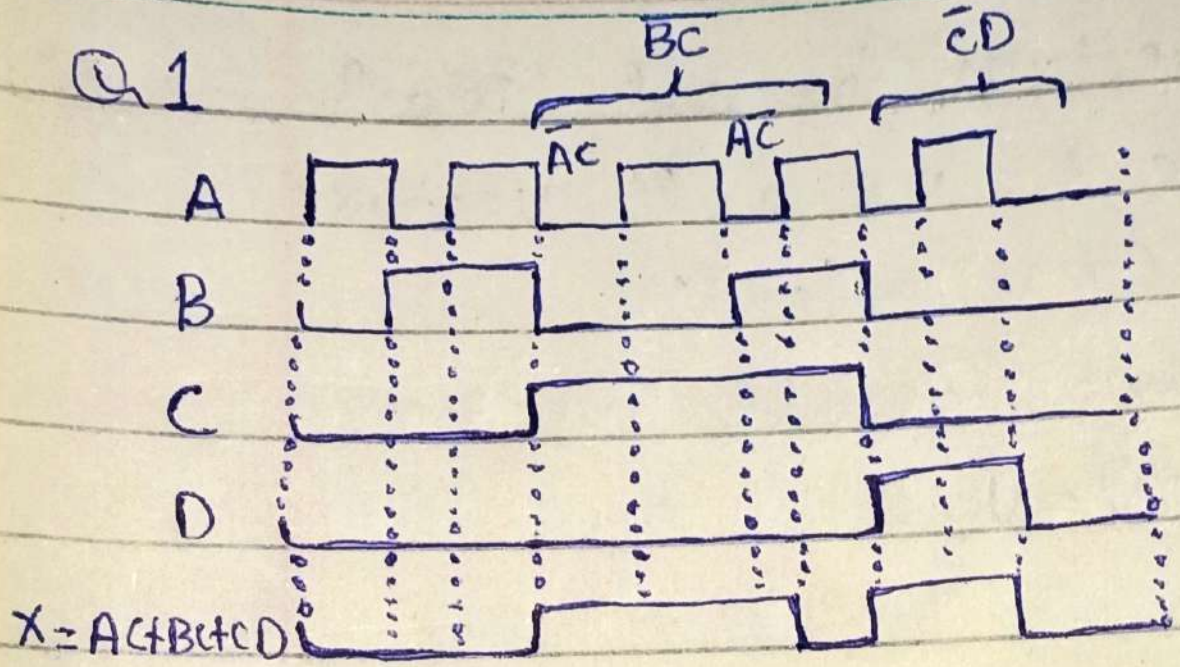
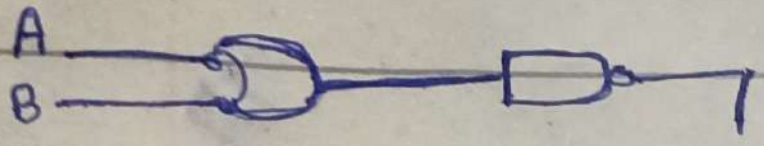
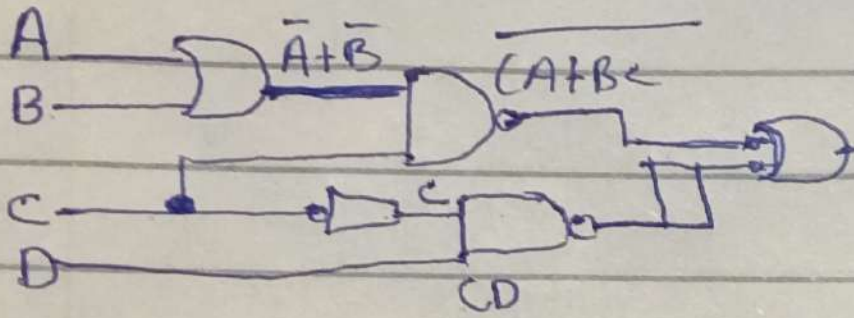
Q1



Solution:

The output expression for the circuit is developed in. The SoP from indicates that the output is High when A is Low and C is High or when B is Low and C is High or when C is Low and D is High.





$X = \overline{(A+B)C + \bar{C}\bar{D}}$

$= (\bar{A}+B)C + \bar{C}\bar{D} =$

$AC + \bar{B}C + \bar{C}D$

$b1 = b2 \oplus g1 = 1 \oplus 1 = 0$

$b0 = b1 \oplus g0 = 0 \oplus 1 = 1$

Binary : 1011

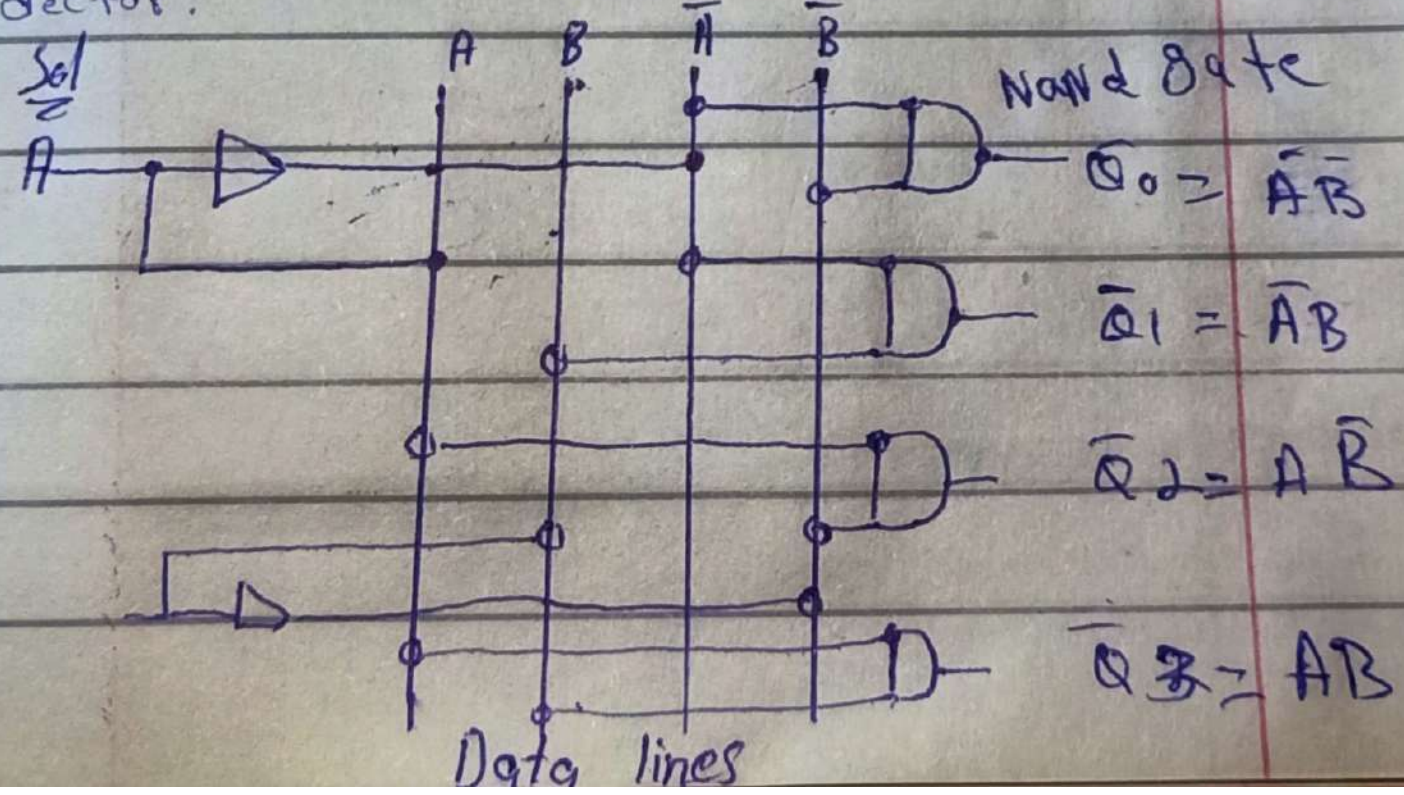
Method 2: (Gray code to binary)

$g3$	$g2$	$g1$	$g0$	Gray code
1	0	1	1	
↓	↓	↓	↓	
1	1	0	1	
$b3$	$b2$	$b1$	$b0$	Gray code
$=g3$	$=b3 \oplus g2$	$=b2 \oplus g1$	$=b1 \oplus g0$	

Binary 1101

06 Draw Logic digram for 4 bit active Lo

decfor.



Now Putting given value and finding output Y

S0	S1	output	Data input
S0=1	S1=0	Y=	D2 = 0
S0=0	S1=1	Y=	D1 = 1
S0=1	S1=1	Y=	D3 = 1
S0=0	S1=0	Y=	D0 = 0

Q5 Show the logic required to convert a 4-bit Gray code to binary and use that logic to convert the following Gray code word to binary 1011

Gray code : 1011

Method 1: (Gray code to Binary)

$b3 = g3 = 1$

$b2 = b3 \oplus g2 = 1 \oplus 0 = 1$

Q2: For the 4-input multiplexer data input are $D=0$, $D=1$ $D2=0$, $D3=1$ Find output y if

$S_0=1$ $S1=0$

$S0=0$ $S_1=1$

$S_0=1$ $S_1=1$

$S_0=0$ $S=0$

Sol. A 4X1 Mux has 4 input lines (D_0, D_1, D_2, D_3) two select input (S_0 ands) and one out Put liney.

if $S, S_0=$ oo then $Y=D_0$

if $S_1 S_0=01$ then $Y=D_1$

if $S_1 S_0=10$ then $Y=D_2$

if $S_1 S_0=11$ then $Y=D_3$

Data input

S_1	S_0	Y
0	0	D=
0	1	D1
1	0	D2
1	1	D3

Q4

Determine the $A = B$, $A > B$, and $A < B$ outputs for the input numbers shown on the comparator in figure 6-22.

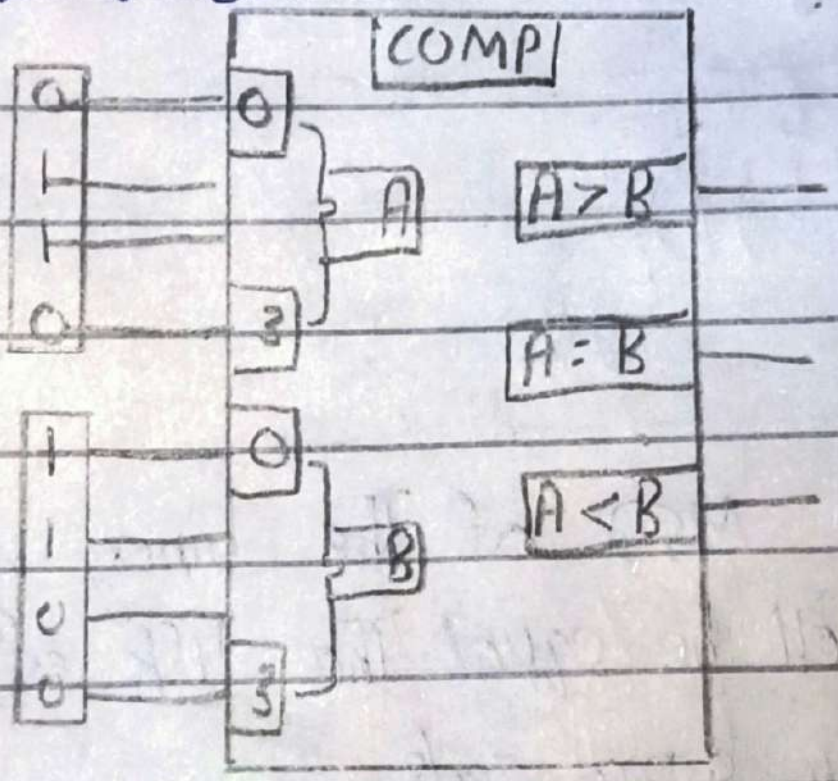


FIGURE 6-22

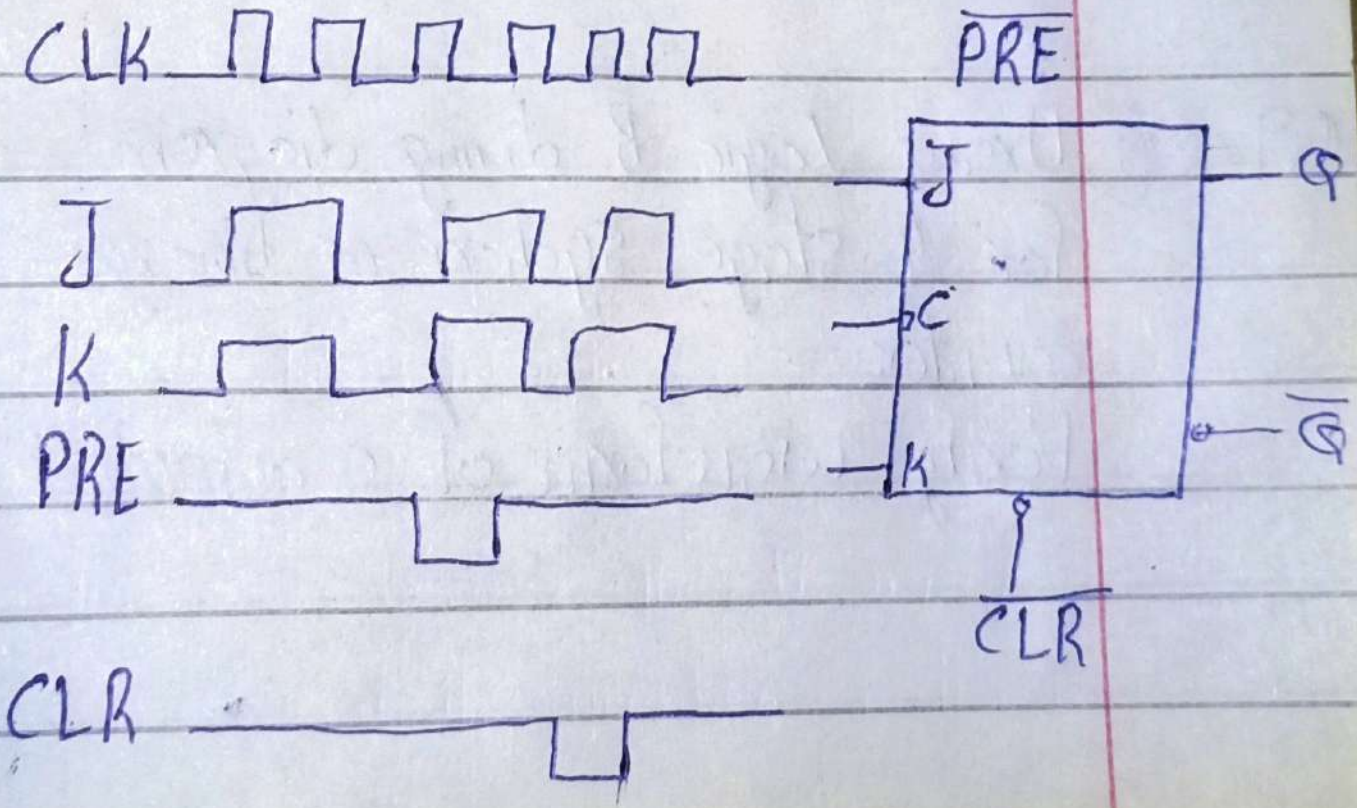
Solution

The number on the A inputs is 01 10 and the number on the B

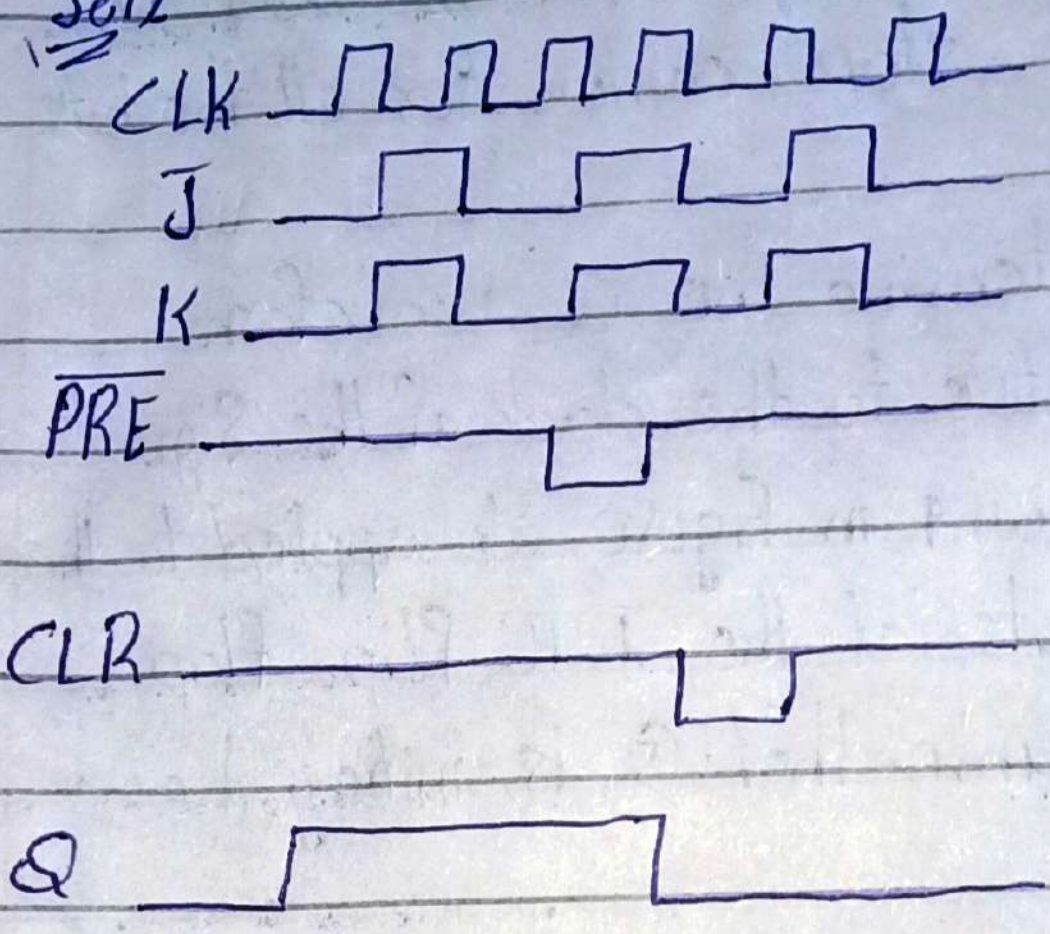
inputs is coll. The A > B output is HIGH and the ~~order or~~ other outputs are LOW.

send binary bit well alter i
(3) The stop canter for all the bits.

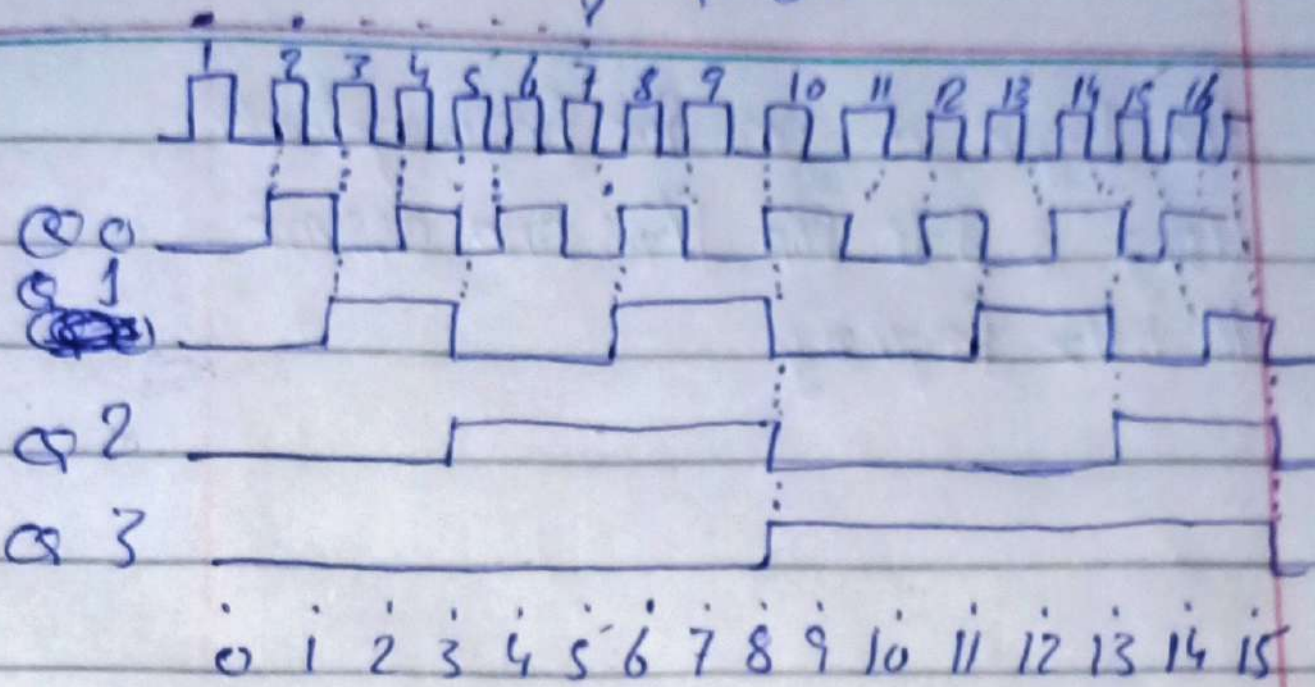
Q8 Determine the Q waveform relative to the clock if the signals showing in Figure 04 applied to the inputs of the J-K flip-flop. Assume that Q is initialy Low.

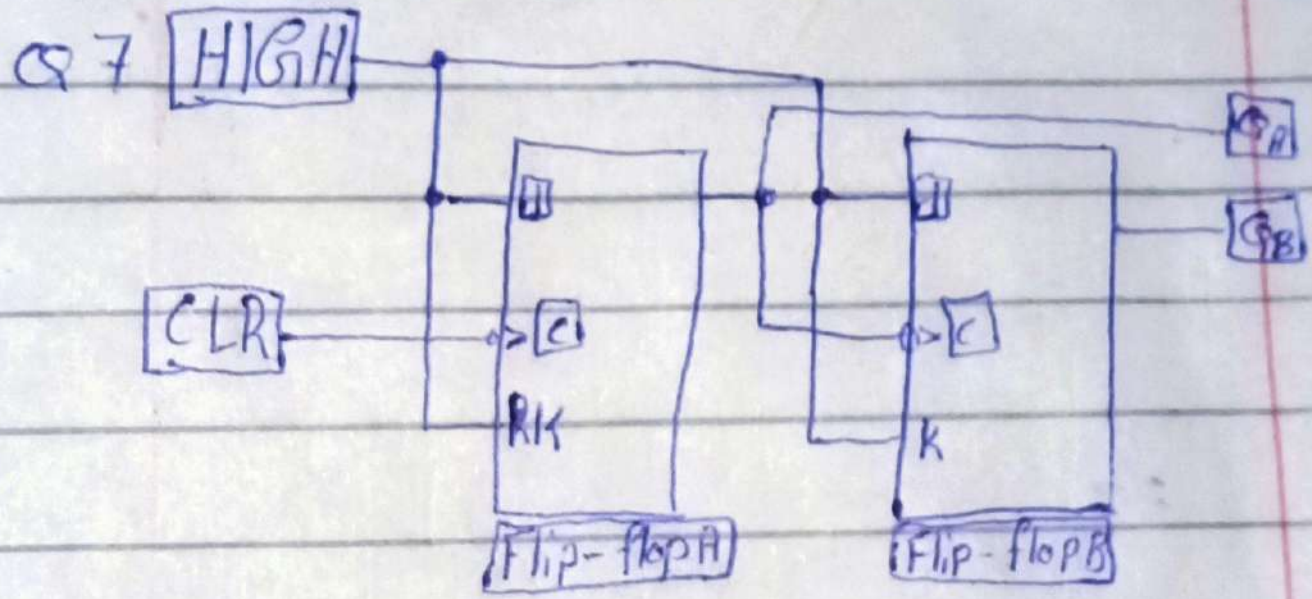


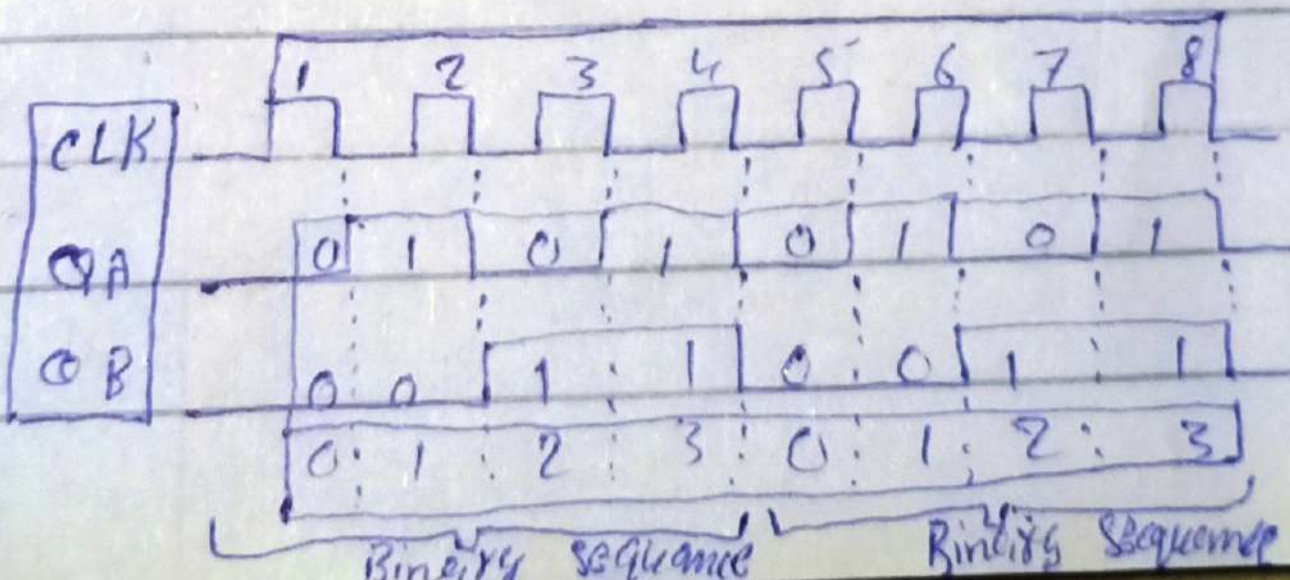
Sol:



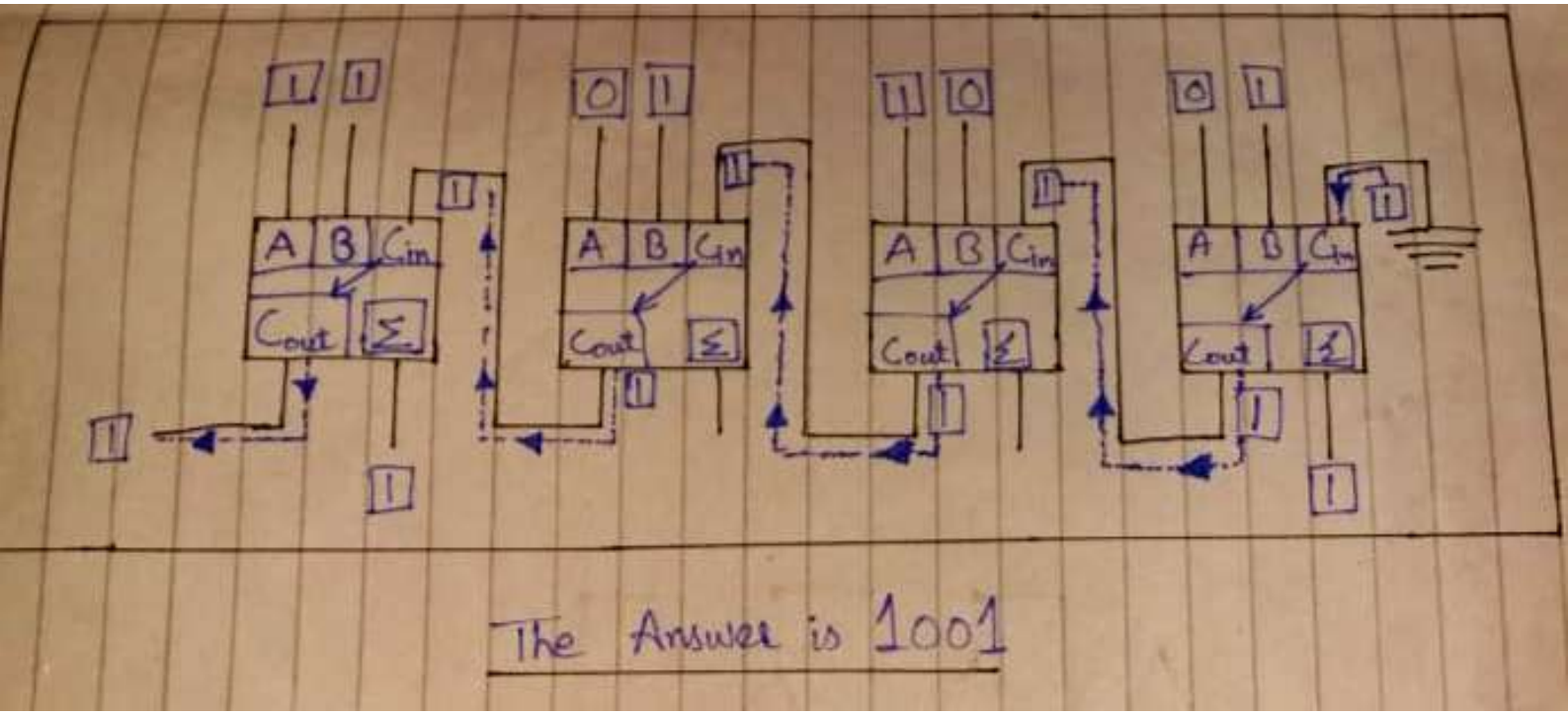
Q9: Draw Logic B diining diagram for 4-stage Sychornous binary counter.
Verify waveform of a output.


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
Q0
Q1
Q2
Q3
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15


Q7
HIGH
CLR
J
C
RK
K
Flip-flop A
Flip-flop B
QA
QB


CLK
QA
QB
1 2 3 4 5 6 7 8
0 1 0 1 0 1 0 1
0 0 1 1 0 0 1 1
0 1 2 3 0 1 2 3
Binary sequence
Binary Sequence

the logic diagram for frequency divider using 3 J-K flip-flops and assume 16 KHz frequency of the initial wave-form. the Negative edge-triggered J-K flip-flops are used for illustration. Both flip-flops are initially Reset. Flip-flops A toggles on the Going transation of each clock Pulse The Q output flif flop A clocks flip flop B So each time Qa makes a High. Shown in the diagram.



The Answer is 1001