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Answer 2

EEPROM

EEPROM stands for electrically erasable programmable read only memory. and it is a type of non-volatile memory used in Computers, integrated in microcontrollers for smart cards and remote keyless systems and other electronic devices to store relatively small amounts of data but allowing individual bytes to be erased and reprogrammed.

Flash memory

flash memory is a type of electronically-erasable programmable read only memory but it can also be a stand alone memory storage device such as USB drive. it is a non-volatile memory chip used for storage and for transferring data.

(2)

Read

information is retrieved from a CD or CD-ROM by a low powerd laser housed in a optical-disk player, or drive unit. The laser shines through the clear polycarbonate while a motor spins the disk past it. The intensity of the reflected light of the laser changes as it encounters a pit.

Write

Recal that on a magnatic disk information is recorded in Concentric tracks. With the simplest constan angular velocity (CAV) system the number of bits per track is constant. An increased in density is achieved with multiple zoned recording in which the surface is divided into a number of zones with zones farther from the center containing more bits than zones closer to the center

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(3)

Parallel-access

All member disks participate inthe execution of every I/O request Typically, the spindles of the individual drives are synchronized so that each disk head is in the same position on each disk at any given time.

independent-access.

Each member disk operates independently so that separate I/O requests can be satisfied.

HD DVD and Blu-ray DVD

HD DVD players have been much cheaper than blu-ray DVD.
Both version deliver sharp resolution
BLUE-ray has 25 GB capacity and is more expensive.
HD-DVD has 15 GB and it is cheaper than Blu-Ray.
But Blu-Ray discs have more storage space and more advance protections against piracy.

④

ANSWER 3

Sequential access.

In this method the memory is accessed in a specific linear sequential manner, like accessing in a single linked list.

Random access.

in this method any location of the memory can be accessed randomly like accessing Array.

Direct access.

In this method the particular location of the memory can be accessed directly like accessing in Array

Associate access

In this memory a word is accessed rather than its address. This access method is a special type of random access method. Application of thus direct memory access is cache memory.

(5)

Principle of locality.

The principle of locality states that data inthe vicinity of a referenced word are likely to be referenced inthe future.

Possible approaches to cache memory.

Bus watching with write through.

Each cache controller monitors the address lines to detect write operations to memory by other bus masters. if another master writes to location in shared memory that also resides inthe cache memory. the cache controller invalidates that cache memory.

Hardware transparancy

Additional hardware is used to ensure that all updates to main memory via controller are reflected in all caches. in addition any matching words in other caches are similarly updated.

(6)

Non-Cacheable memory

only a portion of main memory is shared by more than one processor, and this is designated as non-cacheable. in such system all accesses to shared memory are cache misses, because the shared memory is never copied into the cache. The no_cacheable memory can be identified using chip-select logic or hig-address bits.

Practical issues peculiar to SSDs

SSDs performance has a tendency to slow down as the device is used.

The entire block must be read from the flash memory and placed in a RAM buffer

The entire block from the buffer is now written back to the flash memory.

Flash memory becomes unusable after a certain number of writes

(7)

Front ending the flash with a cache to delay and group write operations.
Using wear-leveling algorithms that evenly distribute writes across block of cells.
Bad block managment technique.

ANSWER 1

Word
The natural unit of organization of memory. The size of a word is typically equal to the number of bits used to represent an integer and to the instruction length.

Addressable
in some system the addressable unit is the word, however many systems allow addressing at the byte level. in any case $2A = N$

Unit of transfer.
For main memory this is the number of bits read out of or written into memory at a time. The unit of transfer need not equal a word or an addressable unit

ANSWER#2(B)

A hard failure is a permanet physical defeat so that the memory cell effected common reliably store data but become stock at 0 or 1. in this context hard failures are errors that occur through process defects and/or circuit bugs-hard failure are repeatable with the corsect sequence of actions within the microcontroller soft errors occur through no failure of the circuit or defect but due to an external source that causes the data to change

ANSWER#1(B)

~~Probability~~ Probably the most effective is least recently used Replace that block inthe set has been inthe cache longest with no reference to it for two-way set associative this is easily implement Each line includes a USE bit. when a line is referenced its USE bit is set to 1 and the USE bit

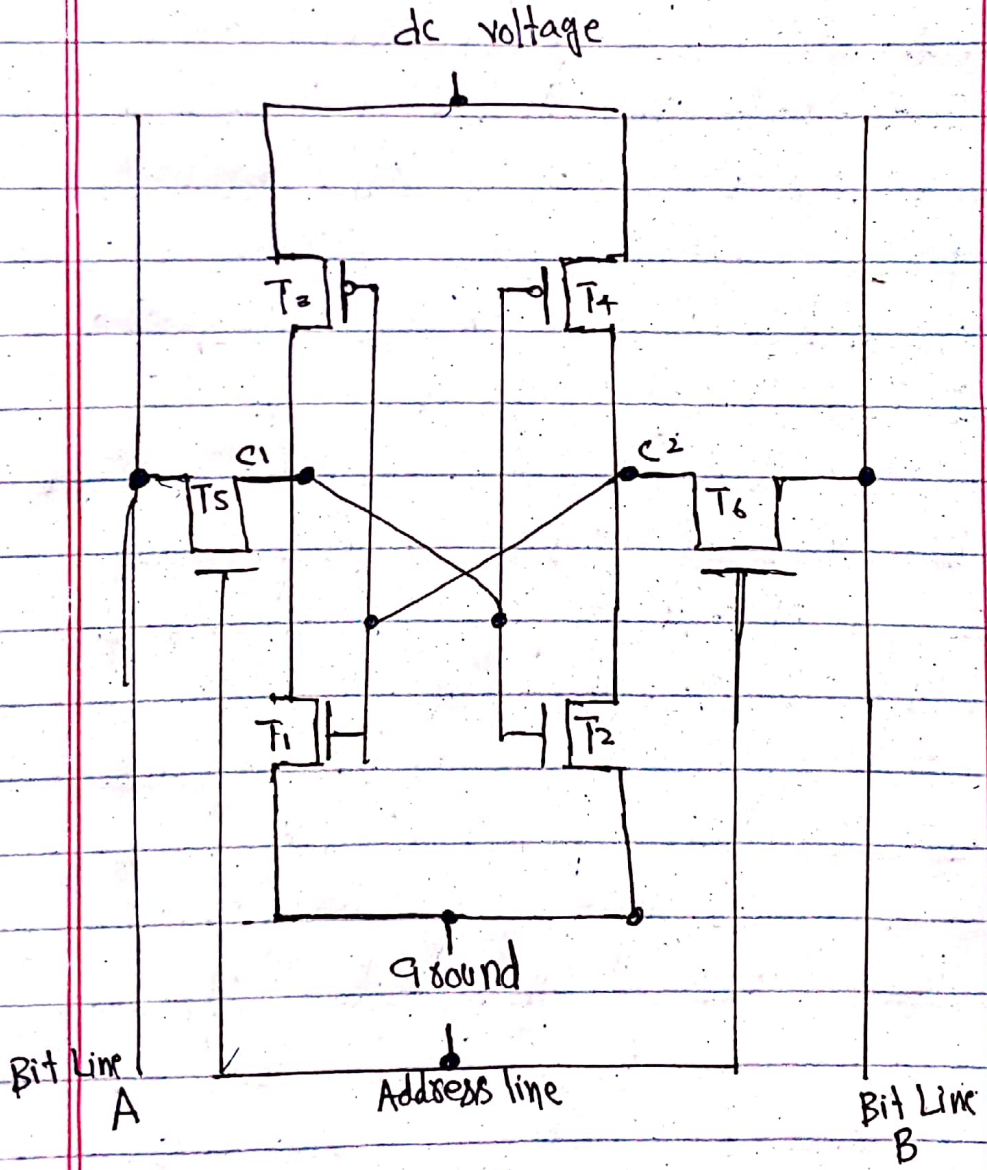
of the other line in that set is set 0. when a block is to be read into the set the line whose USE bit is0used. Because we are assuming that more recently used memory locations are more likely to be referenced, LRU should given the best Hit ratio LRU is also relatively easy to emplement for a fully associative cache. still another possibility is least frequency used. Replace that block inthe set that has experienced the fewest refrences. LFU could be implemented by associating a counter with each line. A technique not based on usage. not LRU, LFU, FIFO or some variant is to Pick a line at random from among the candidate lines. Simulation studies have shown that random replacement provides only slightly inferior performance to an algorith based usage.

Read operation

In SRAM for any operation to be performed the word line should be high to perform read operation initally

Write operation

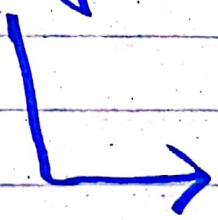
Consider the memory bits consists of Q=0 and Q=1



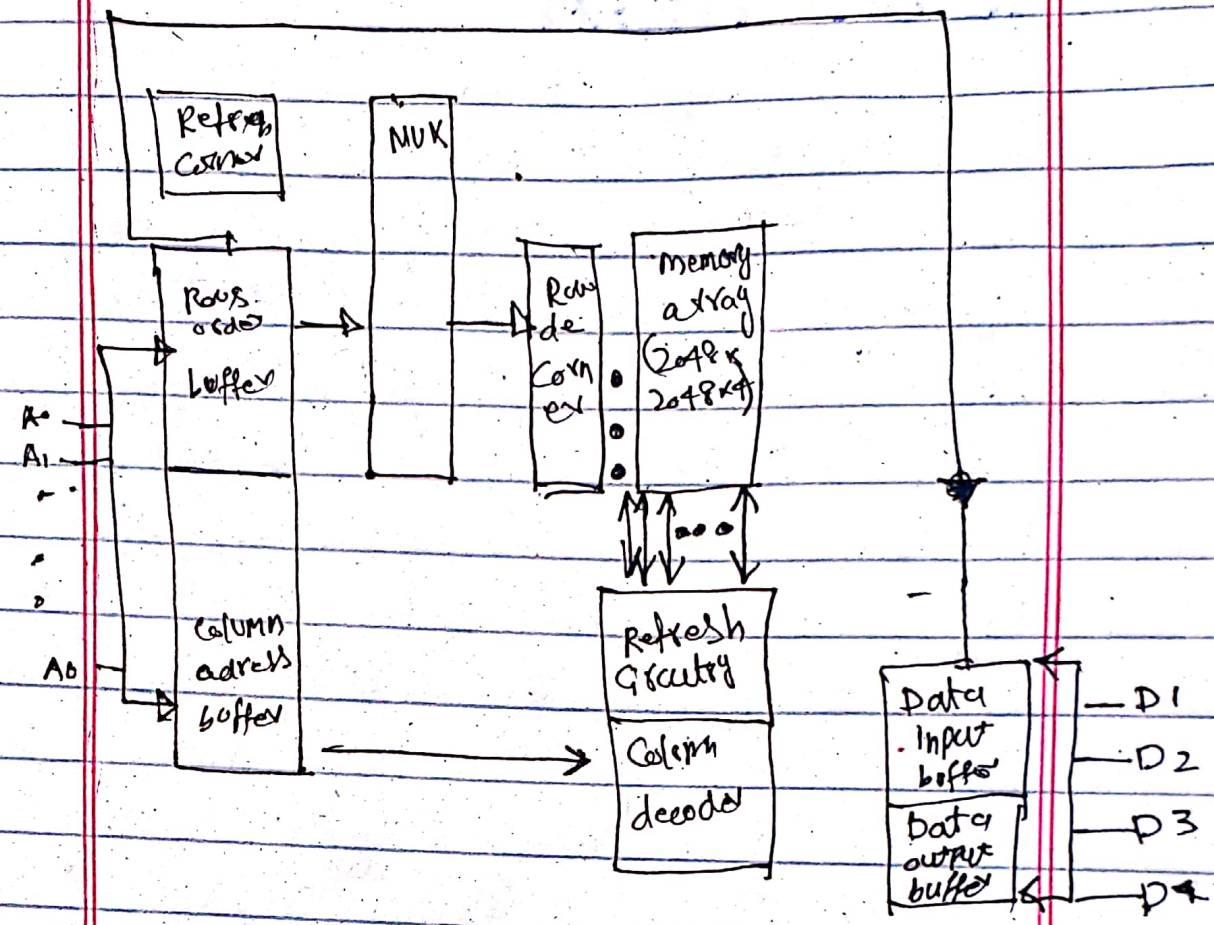
16 Bit DRAM

In this case 4 bits are reads or written at a time logically the memory array is organized as four sequre arrays of 2048 by 2048 elements. various physical arrangments are possible In any case the elements ar possible. in any case the elements are the array are connected by both horizontel and vertical lines. Because only 4bits are read/written to this DRAM there must be multiple DRAM connected to the memory Contboller to read/write a word of data to the bus

Diagram



(12)



Reason for DVD's greater capacity over CD

Bits are packed more closely on a DVD. The spacing between loops of a spiral on a CD is 1.6 μm and the minimum distance between pits along the spiral is 0.834 μm. The DVD uses a laser with shorter wavelength and achieves a loop spacing of 0.74 μm and a minimum distance between pits of 0.4 μm. The decoder

result of these two improve ments is about a seven-fold increases in capacity, to about 4.7 GB the DVD employs a second layer of pits and lands on top of the first layer and by adjusting focus the layer in DVD drives can read each layer separately.

ANSWER 4(b)

Total block inthe cache = 8k bytes

16 bytes $= 2^3 \times 2^{10} / 2^4 = 2^9 = 512$

Number of set = number of block in cache/2

Number of set = 512/2

Number of set in cache = 256

Number of set in cache $= 2^8$

Number of set = 8

No of set = 8

Size block = $16 = 2^4$

Size of memory $= 2^6 \times 2^{20} = 2^{26}$

Tag = size of memory - set - size of block

Tag = 26 - 8 - 4 $\Rightarrow$ 14

Tag	set	size of block
14	8	4

(14)

ANSWER 4(a)

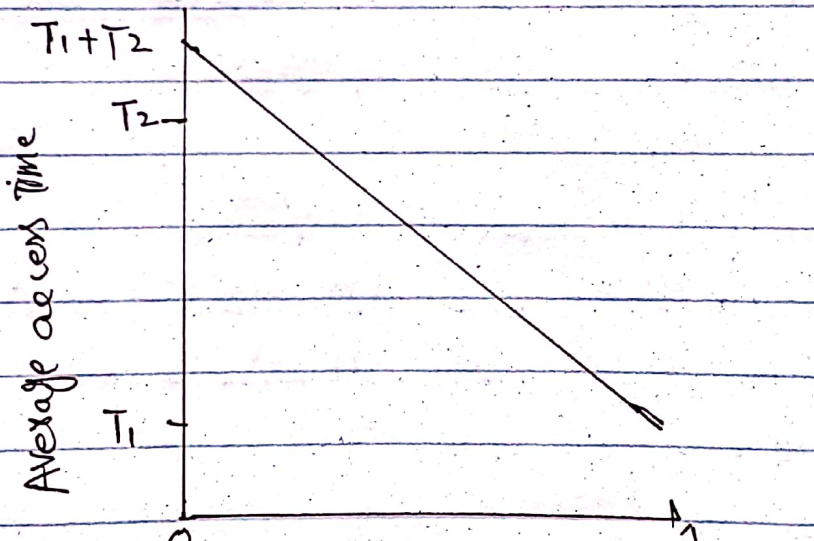
in example Suppose 95% of the memory accesses are found in level 1. Then the average time to access a word can be expressed as

~~(0.95)(0.01MS)+(0.05)(0.01MS)~~

$(0.95)(0.01MS)+(0.05)(0.01MS+0.1MS)$

$= 0.0095 + 0.0055$

$= 0.015MS$



(15)

ANSWER 4(D)

72 revolution in 60 sec

1 revolution in 60/720 OR

1 revolution in 6ms

1 revolution = covering one entire track = 500 sector

500 Sector = 6ms

1 Sector = 8 microsecond

1.28MB = 1342177.28 Bytes

OR 2621.44 Sector = 2622

Sector = 20.970 ms

Total time case

Case (1) 4+2+20 = 26ms

Case (2) 4+2+20.976 = 26.976ms

ANSWER (C)

M = 8

$2^{k-1} >= k+M$

$2^{4-1} >= 4+8$

$15 >= 12$