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Assignment : no 2

Subject : Digital Logic Design

Course code(CS): CSC-201

EDP Code (CS) : 1020020777

Assignment No : 3
Name : Ingun ullah
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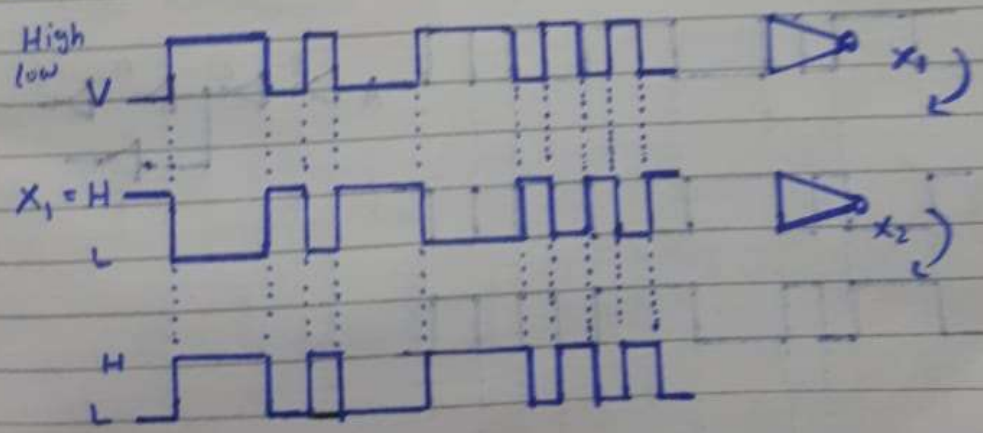
Subject : DLD

Program : BC CS

Q1. The input waveform in figure is applied to a system of two inverters connected in series Draw the output waveform across each inverter in Proper relation to the input.

Sol



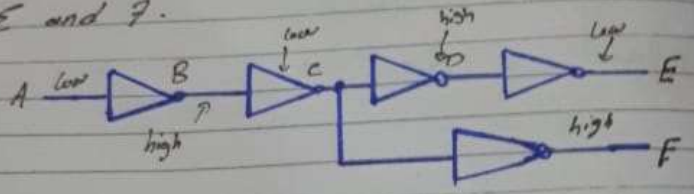
Q4: Deter
AND
shown

Sol:-

X=

Q3:- A Combination of inverters is shown in Figure 02. If a low is applied to Point A determine the resultant output at Points E and F.

Sol:-



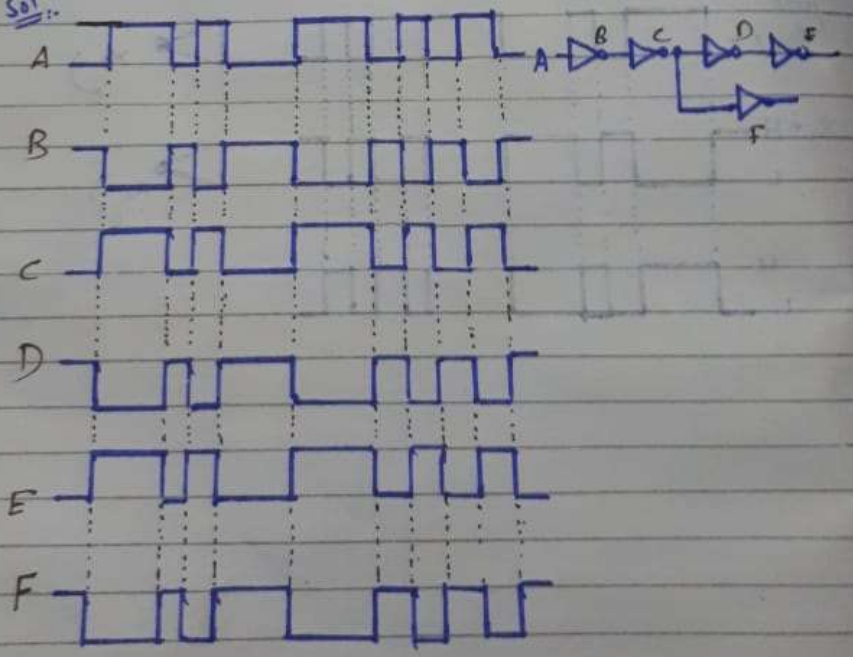
E = low

F = High

Q5:- To g

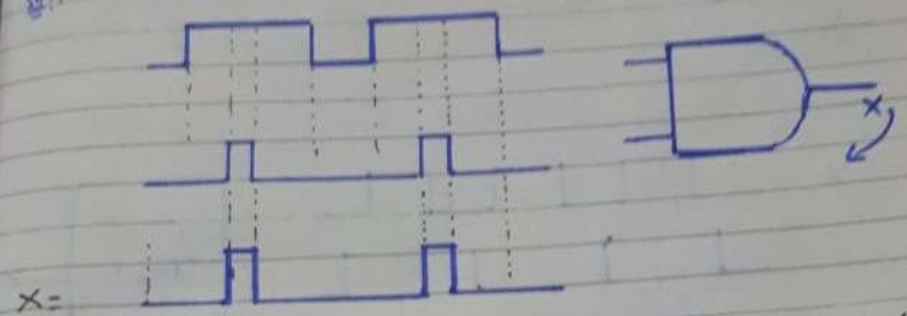
Q3:- If the waveform in Figure 01 is applied is applied to Point A in Figure 02 determine the waveforms at Points B through F.

Sol:-

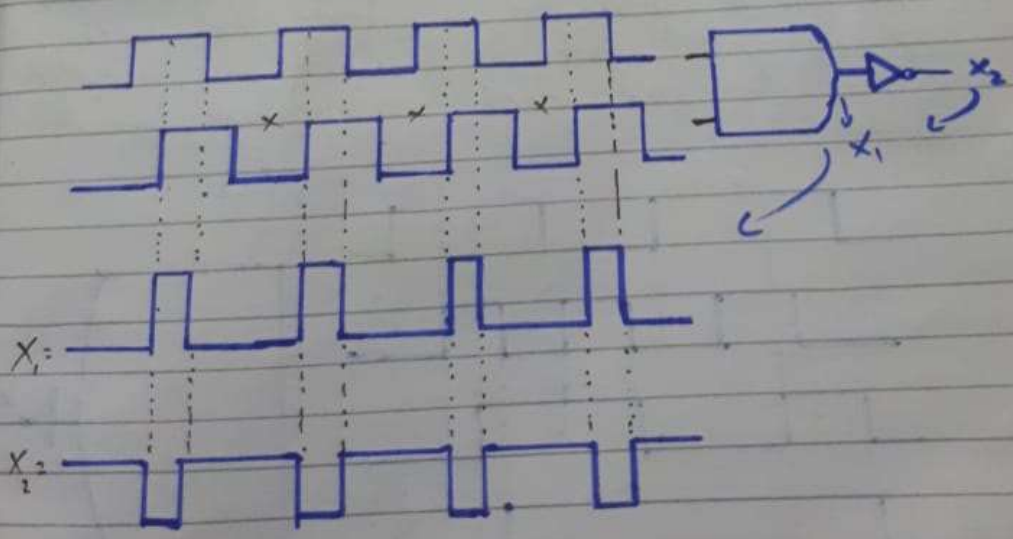


Q4. Determine the output x, for a 2 input AND gate with the input waveforms shown in figure.

Sol:-

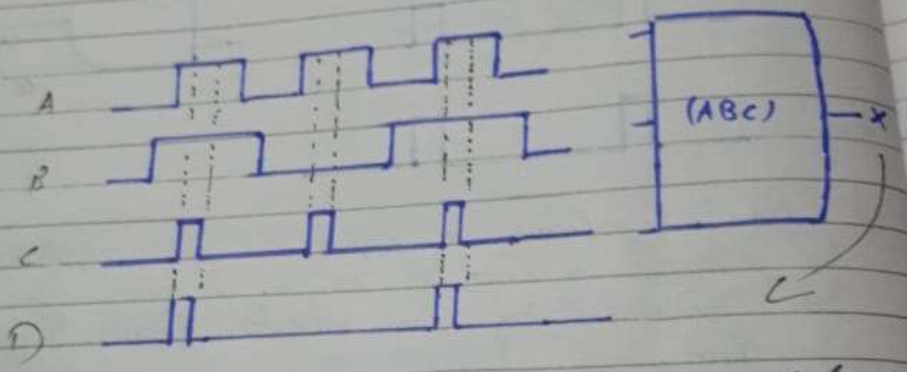


Q5:- The waveforms in figure. 04 are applied to points A and B of a 2-input AND gate followed by an inverter. Draw the output waveform.

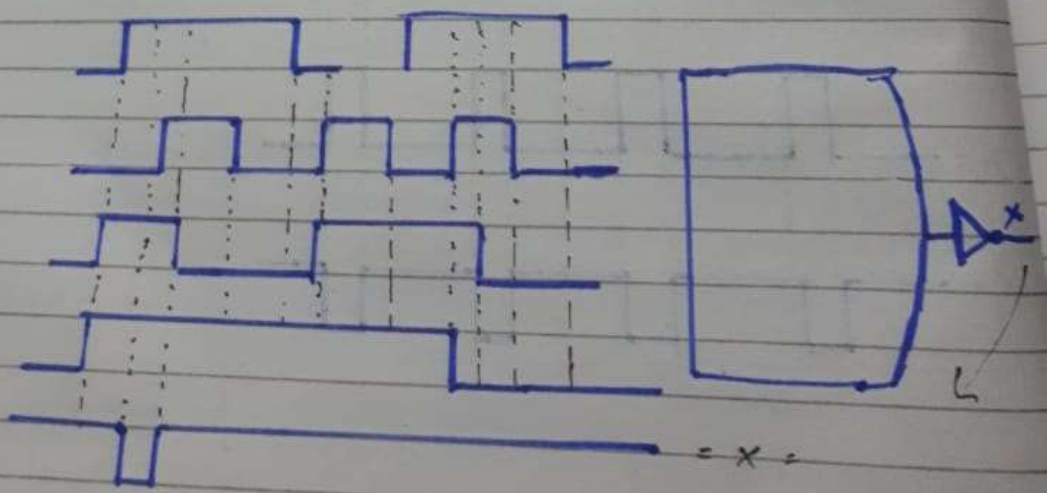


Q6: The input waveforms applied to a 3 input AND gate are as indicated in figure show the output waveform in proper relation to the inputs with a timing diagram.

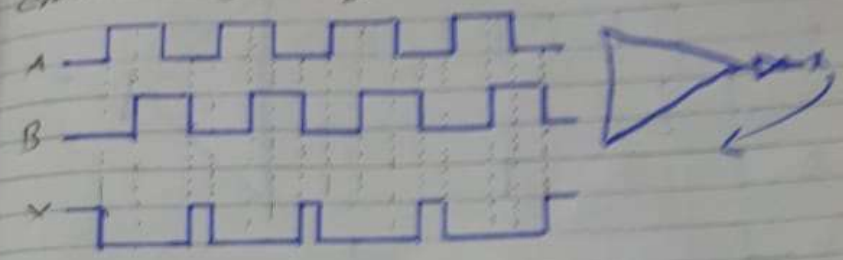
Sol:



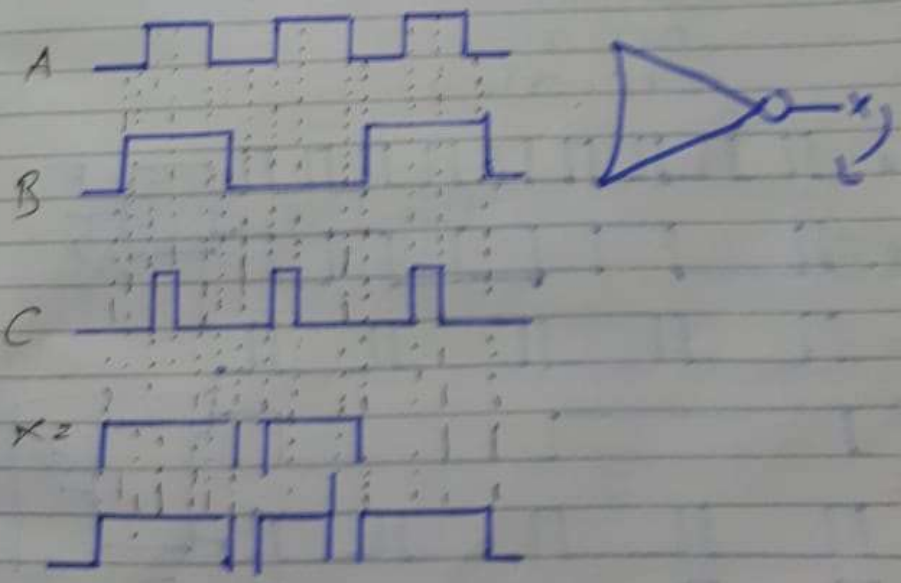
Q7: The input waveforms applied to a 4 input AND gate are as indicated in figure The output of the AND gate is fed to an inverter Draw the net output waveform of this system.



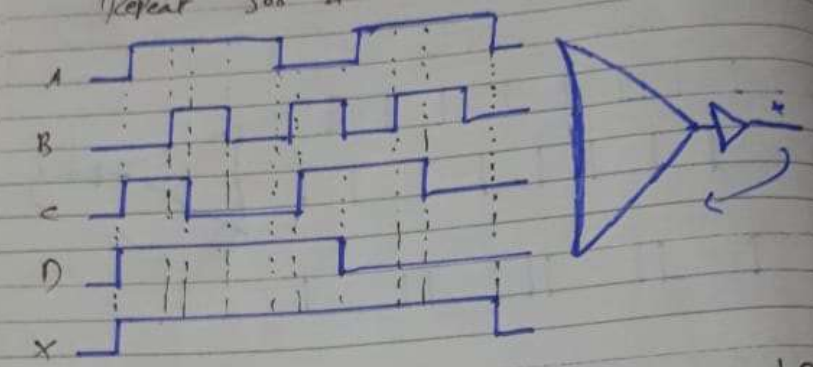
Q8) Determine the output for a 2 input OR gate when the input waveforms A and B are given and draw a timing diagram.



Q9 Repeat for a 3-input OR gate.

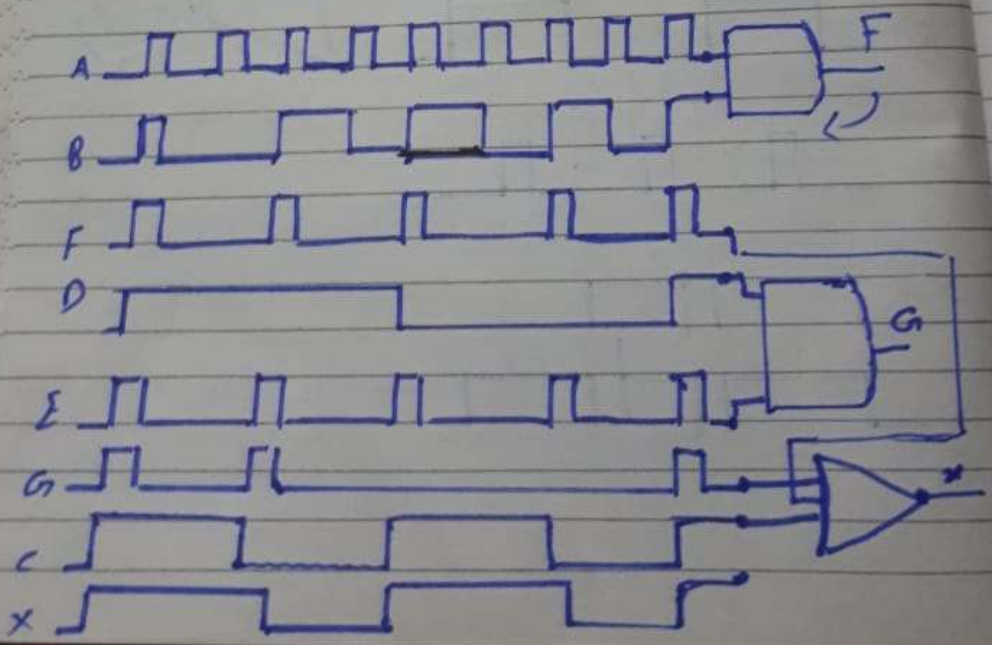


Q10 Repeat for a 4 input OR gate.



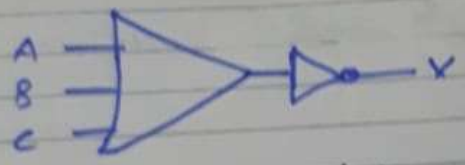
Q12 For the waveforms given in A and B are ANDed with output F. D and E are ANDed with output G and C, F and G are ORed Draw the net output waveform Q13

Ans (AB) = F
(DE) = G
(C + F + G) = X.

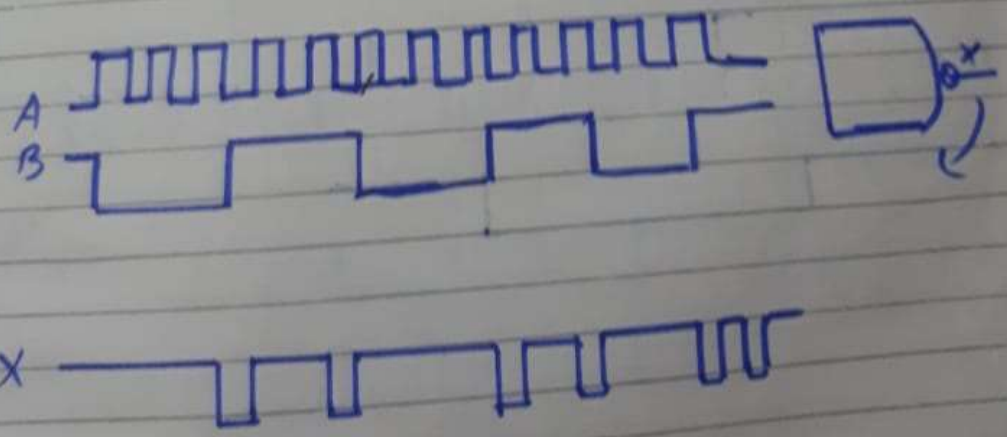


Q12 Show the truth table for a 3 input AND gate followed by an inverter.

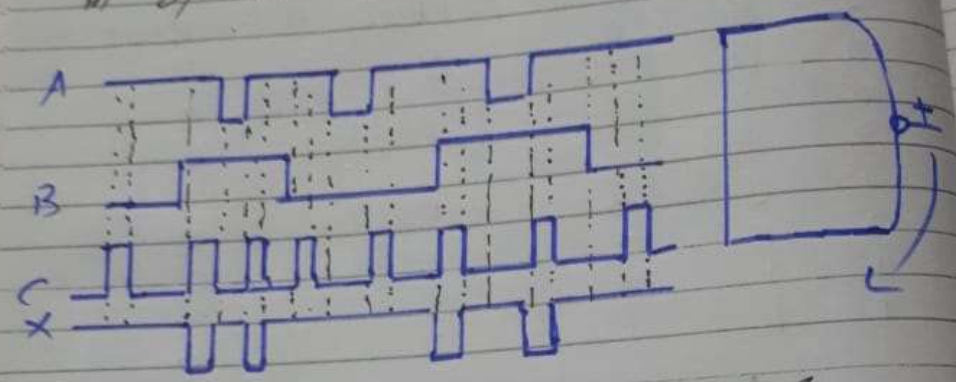
A	B	C	(A·B·C)	$\overline{(A \cdot B \cdot C)}$
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0



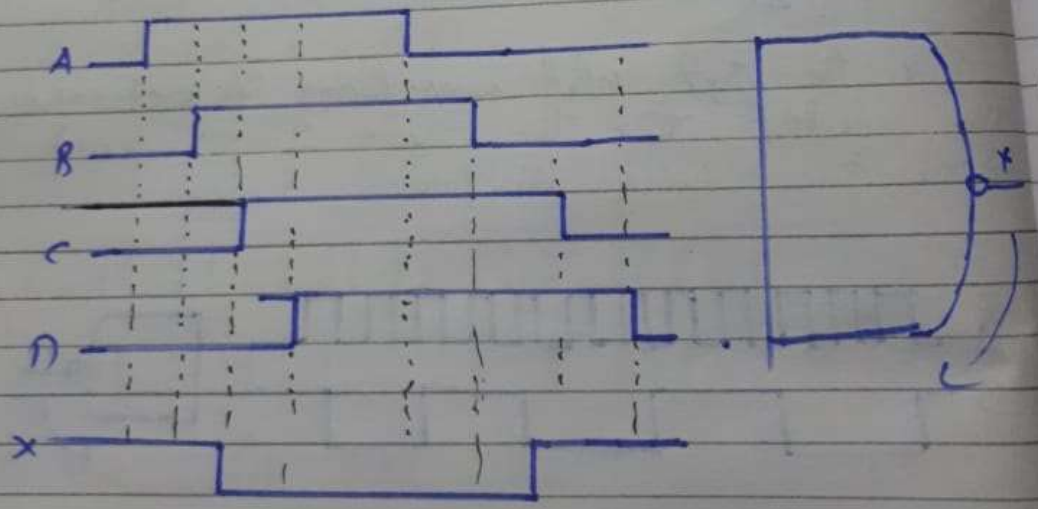
Q13 For the set input waveforms in determine the output for the gate shown and draw the timing diagram.



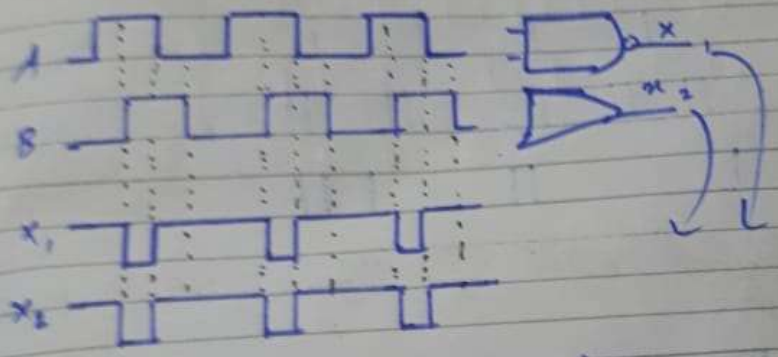
Q14 Determine the gate output for input waveforms in of and draw the timing diagram.



Q15 Determine the output waveform in figure 10

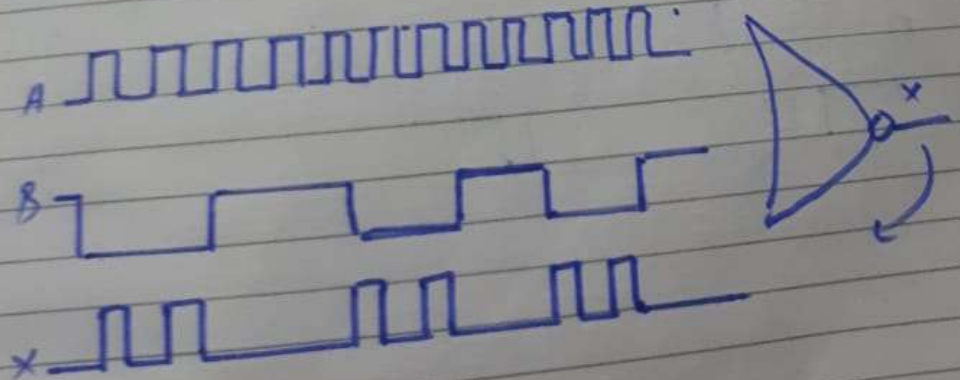


Ans The two logic ~~Sym~~ Symbols shown in represent equivalent operation. The difference between the two is strictly form a functional viewpoint for the NAND Symbol work ..... the same output for the given inputs.

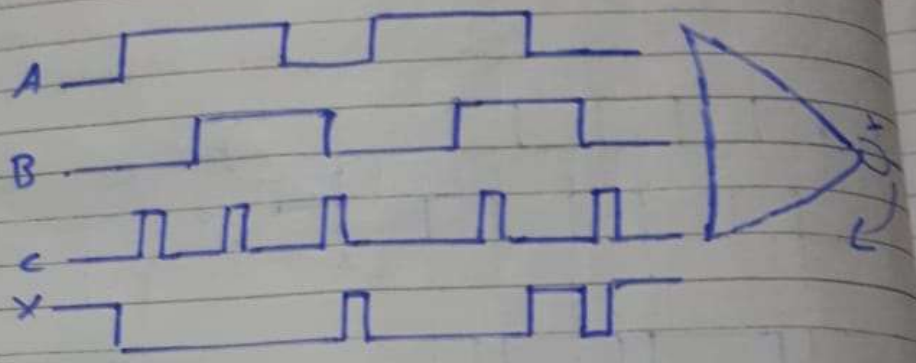


Q17 ~~Determine the output waveform in Figure.~~

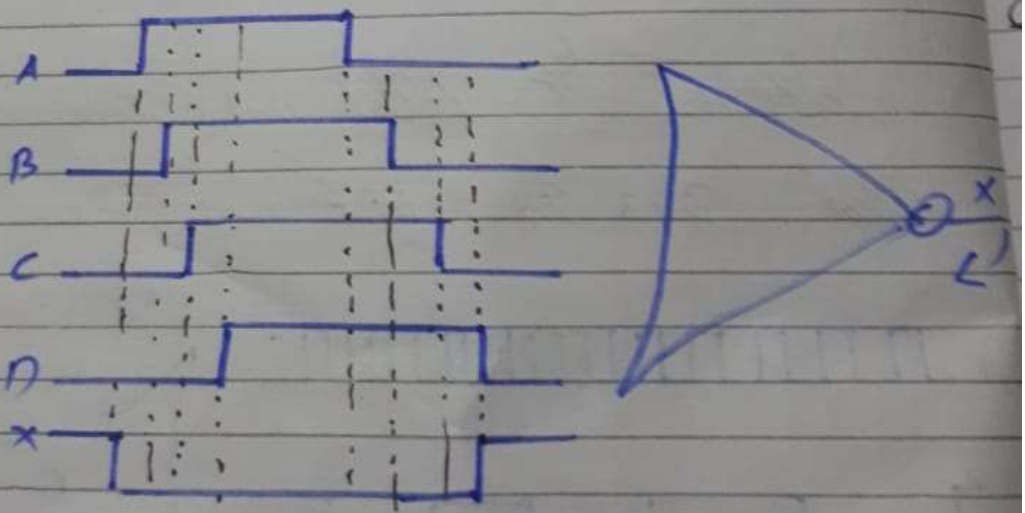
Refer Q13 for 2 input NOR gate.



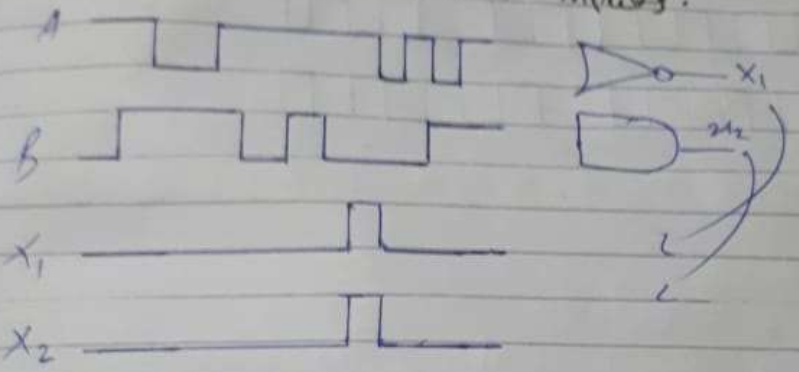
Q18 Determine the called waveform in figure and draw the timing diagram.



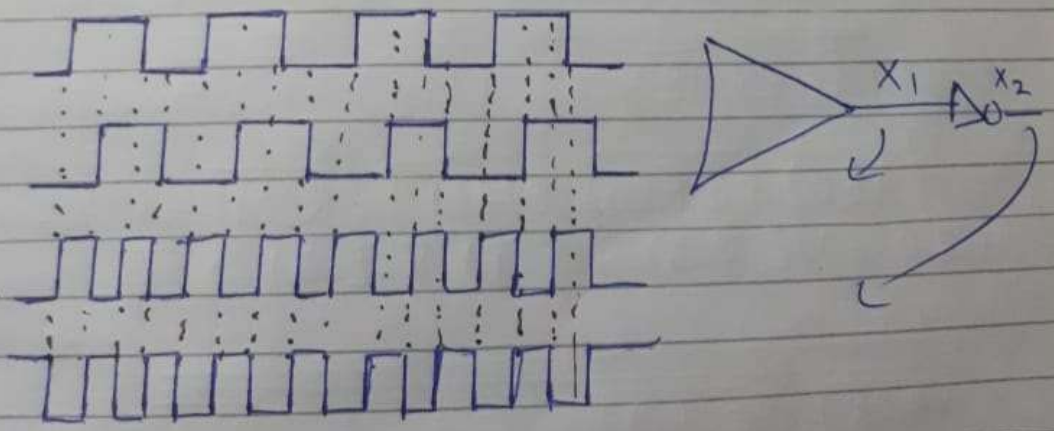
Q19 Repeat Q15 for four input NAND gate



(c) The NAND and the negative - OR symbols represent equivalent operation but they are functionally different for HIGH..... Figure 12 will produce the same output for the given inputs.



Q24 Redraw Q5 for an exclusive OR gate



Case Related to Ex-OR gate
XOR Gate.