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Attempt all questions

Q NO # 1

Give answer to each of the following

Part (a)

word:-

The natural unit of organization of memory. The size of word is typically equal to the number of bits used to represents an integer & to the instruction length.

Addressable unit

In some systems the addressable unit is the word. However many systems allow addressing at the byte level. In any case 2A = N.

* **unit of transfer**

For main memory this is the number of bits read out of or written into memory at a time. The unit of transfer need not equal a word or an addressable unit.

part (b)

probabably the most effective is least recently used (LRU): Replace that block in the set that has been in the cache longest with no reference to it. For two-way set associative this is easily implemented. Each line included a use bit. When a line is referenced its use bits is set to 1 & the use bit of other line in that set is set to 0 when a block is to be read into the set, the line whose use bit is 0 is used. Because we are assuming that more recently used more memory location are more likely to be referenced LRU should give the best hit ratio. LRU is also relatively easy to implement for a fully associative cache. The cache mechanism maintains a separte list of indexes to all the lines in cache when a line is referenced it moves to the front of the list for replacement the line at the back of the list is used. Because of the its simplicity of most popular

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replacement algorithms

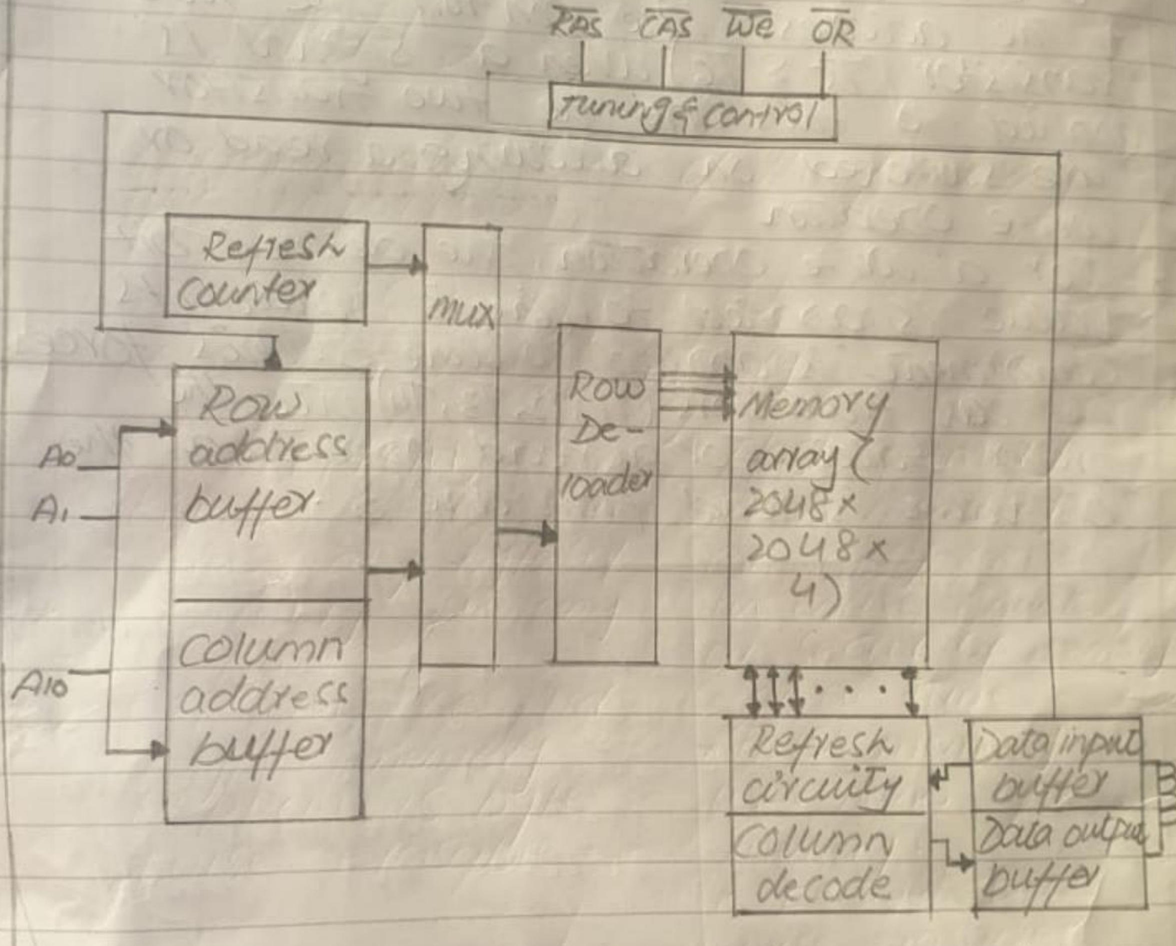
* Still another possibility is least is least frequently used (LFU): Replace that block in the set that has experienced the fewest reference. Lfu could be implemented by associating a counter with each line. A technique not based used usuage (i.e, not LRU, LFU, FIFO or some variant) is to pick a line that at random from among the candidate lines. Simulations studies have shown that random replacement provides. Only slightly inferior performances to an algorithms based on usuage [SMIT82].

part (c)

The SRAM address line is used to open or close a switch.
* The address line controll the two transistor (T5 & T6) when a signal is applied to this line the two transitor are switched on allowing a read or write operation
* For a write operation, the desired bit value is applied to line B while its compliment is applied to line B. This forces the four transistors (T_1, T_2, T_3, T_4) into the proper states. For a read operation the bis value is read from line B.

part (D)

Discuss 16-M Bit DRAM (4M x 4) organization in detail:



TYPICAL Megabit DRAM (4MX4)

Because only 4bits are read/written to their DRAM there must be multiple DRAM connected to the memory controller to read/written a word of data to the bus. All the DRAMS require a refresh operation. A simple technique for refreshing is in effect to disable the DRAM chip while all the data cells are refreshed. The refresh counter steps through all of the row values his causes each cells in row to be refresh.

part (e)

What are the reasons for Dvd's greater capcity over CD?

A Reasons for DVD's greater capcity over CD :-

The Dvd's greater capcity is due to three difference from CDs:

1) Bits are packed more closely on a Dvd. The Spacing between loops of a Spiral on a CD is 1.6 µm & the minimum distance between pits along the Spiral is 0.834 µm. The DVD uses a laser with Shorter wavelength & acheive a loop spacing of 0.74 µm & a minimum distance between pits of 0.4 µm. The result of these two improvements is about a Seven fold increase in capcity to about 4.7GB.

2) The DVD employs a Second layer of pits & lands on the top of the first layer. A dual layer DVD has a Semi-reflective layer on the top of the reflective layer & By adjusting focus, the laser in DVD drives can read each layer Separtely. This technique almost double the capcity of the disk to about 8.5GB. The lower reflective of the Second layer limits its stoarge capcity So that a full doubling is not acheived.

3) The DVD rom can be two sided. wherea

data are recorded on only one side of a CD. This bring total capcity upto 17GB.

QNO# 2

Differentiate each of the following in detail:-

part (a)

EEPROM & Flash memory

EEPROM	Flash memory
* EEpROM device can erase any byte of memory at any time	* Flash memory can only erase an entire chunk or sector of memory at a time.
* EEPROM uses nor type memory	* Flash memory uses nand type memory.
* EEPROM is byte wise erasable.	* Flash is block wise erasable.

Part (B)

* hard failure

A hard failure is a permanent physical detect so that the memory cell or cell affected cannot reliably store data but become stuck at 0 or 1 switch erratically between 0 & 1. Hard error can be caused by harsh environmental abuse, manufacturing defects & wear.

* Soft error:-

A soft error is a random non-destructive event that alters the contents of one or more memory cells without damaging the memory. Soft error can be caused by ~~error~~ power supply problems or alpha particals. These particals result from radioactive decay & are distressingly common because radioactive nuclei are found in small quantities in nearly all materials. Both hard & soft error are clearly undesirable & most modern main memory systems include logic for both detecting & correcting errors.

Part (c)

Read & write mechanism for magnetic disk

* **Magnetic disk read & write mechanism:-**

* **Read:-**

The traditional read mechanism exploits the fact that a magnetic field moving relative to a coil produces an electrical current in the coil. when the Surface of the disk passes under the head. it generates a current of the same polarity as the one already recorded. The Structure of the head for reading is in this case essentially the same as for writing & therefor the same head can be used for both such single heads are used in floppy disk Systems & in order rigid disk system. contemporary rigid disk systems use a different read mechanism requiring a Separate read head postioned for Convenience close to the write head. The read has consist of partially Sheilded magnetorestive (MNR) Sensor. The MR material has an electrical resistance that depend on the direction on the magnitization of the medium moving under it. By a passing a current through it. By passing a current through the MR Sensor, resistance changes are detected as voltage signals. The MR design allows high-frequency operation, which evuates to greater Stoarge densities & operating speeds.

* Write:-

The write mechanism exploits the fact that electricity flowing through a coil produces a magnetic field. Electric pulses are sent to the write head, & the resulting magnetic patterns are recorded on the surface below with different patterns for positive & negative currents. The write head itself is made of easily magnetizable material & is in the shape of a rectangular doughnut with a gap along one side & a few turns of conducting wire along the opposite side. An electric current wire induces a magnetic field across the gap which in turn magnetize a small area of recording medium. Reversing the direction of the current reveses the direction of the magnetization on the recording medium.

part (D)

D) Parallel access & independent access RAID Schemes

* Parallel access:-

All member disk participate in the execution of every I/O request. Typically the spindles of the individuals drives are synchronized so that each disk head in the same postion on each disk at any given time.

* **independent access:-**
Each member disk operates independently so that separate I/O requests can be statisfied in parallel.

part (e)

e) HD DVD & Blu ~~DVD~~ ray DVD.

* HD DVD players have much been cheaper than Blu-ray machines, But Blu-ray disc have more stoarge space & more advanced protection against piracy.
* Both version deliver sharp resolution.
* Blu-ray has 25GB capacity (50GB for dual layer) & is more expensive.
* HD-DVD has 15GB (30GB for dual layer) & is cheaper than Blu-ray.

QNO#3

part (a)

a) Memory access methods

Memory Access Method:-
There are 4 types of memory access methods:-

1) **Sequential Access:-**
In this method, the memory is accessed in a specific linear sequential manner like accessing in a single linked list. The access time depends on the location of the data. Application for sequential memory access are magnetic tapes, magnetic

disk & optical memories.

* **Random Access:-**

In this method of any location of the memory can be accessed randomly like accessing in array physical location are independent in this access method. Application for this random memory access are Ram & Rom.

* **Direct Access:-**

In this method, the particular location of the memory can be accessed directly like accessing in array. This method is a combination of above two access methods. The access time depend on both of the memory organization & characteristics of stoarge technology. The access is semi-random or direct.

* **Associative access:-**

In this memory, a word is accessed rather than its address. This access method is a special type of random access method. Application of thus direct memory access is cache memory.

part (B)

b) principal of locality
* The principal of locality states that data in vicinity of a referenced word are likely to be referenced in the near future.

part (C)

c) possible approches to cache coherency:-

possible approches to the cache coherency include the following

* Bus watching with write through:-

Each cache controller monitor the address line to detect write operation to memory by other bus masters. if another master write to a location in shared memory that also reside in the cache memory, the cache controller invalidates that cache entry. This strategy depend on the use of a write-through policy by all cache controllers

* Hardware transparency:

Additional hardware is used to ensure that all updates to main memory via cache are reflected in all cache, this update is written in main memory, In addition any matching words in other caches are similarly updated.

* Non-cacheable memory

only a portion of a main memory is shared by more than one processor, & this is designated as non-cacheable. In such a system all access to shared memory are cache misses, because the shared memory is never copied into the cache. The non-cacheable memory can be identified using chip-select logic or high-address bits.

part (D)

d) practical issues peculiar to SSDS

There are two pratical issues peculiar to SSD'S that are not faced by HDDS

* SSD performance has a tendency to slow down as the device is used
* The entire block must be read from the flash memory & placed in a RAM buffer.
* Before the block can be written back to flash memory, the entire block of flash memory must be erased.
* The entire block from the buffer is now written back to flash memory

* Flash memory becomes unusable after a certain number of writes.
* Techniques for prolonging life:-
* Front ending the flash with a cache to delay & group write operations
* Using wear-leveling algorithms that evenly distribute write across block of cells
* Bad-block mangement techniques.
* Most flash devices estimate their own remaining life time. So system can anticipate & take preemtive action.

Part (e)

CD read & write operation

* Read
information is retrived from a CD or CD rom by a low powered laser housed in an optical disk player or drive unit. The laser shines through the clear polycarbonate while a motor spins the disk past it. The intensity of the reflected light of the laser changes as

it encounters a pit. Specifically if the laser beem falls on a pit which has a Somewhat rough Surface, the light Scatters & a low intensity is reflected back to the Source. the area between pit are called land. A land is a Smooth surface. which reflects back at higher intensity. The change between pit & land is detected by a photo Sensor & converted into a digital Signals The Sensor test Surface at regular intervals The begining or end of a pit represents a 1; when no change in elevation occurs between intervals a 0 is recorded.

* Write

Recall that on a magnetic disk, information is recorded in concentric tracks with the Simplest constant angular velocity (CAV) System. the number of bits per track is constant An increase in density is acheived with multiple zone recording in which the Surface is divided into the number of zones with zones farther from the centre Containing more bits than zones closer to the Centre. Although this technique increases capcity. its still not optimal.

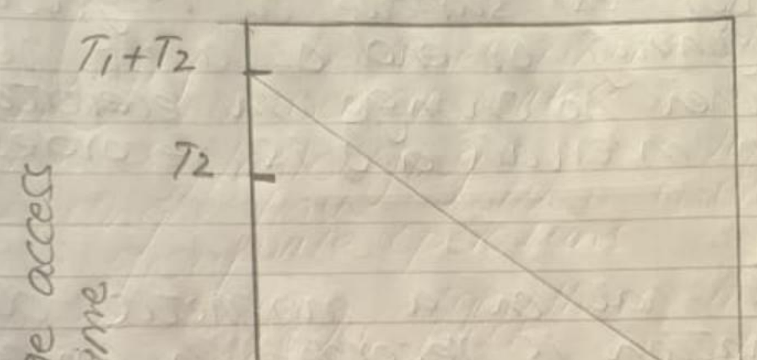
Q NO # 4

Part (a)

In our example Suppose 95% of the memory access are found in level 1 Then the average time to access a word can be expressed as

$(0.95)(0.01\mu s)+(0.05)(0.01\mu s+0.1\mu s)=0.0095+0.0055=0.015\mu s$

The average access time is much closer to 0.01 μs than to 0.01 μs are desired.



Fraction of access involving only level 1 (hit ratio)

Part (b) * TAG Set & Word:-

Total block in the cache = 8K bytes/16bytes = $2^3 \times 2^{10}/2^4 = 2^9 = 512$

Number of Sets = number of block in Cache/2

Number of Sets = 512/2

Number of Sets in cache = 256

Number of Sets in cache = 2^8

Number of Set = 8

- Size of block = $16 = 2^4$
- Size of memory - Set size of block
- Tag = 26 - 8 - 4
- Tag = 14

Tag	Set	Size of block
14	8	4

Tag (9) / Set (B) / word (2) 177H/0EEH/3H

part (C)

M = 8

$2^k - 1 \geq k + m$

$2^4 - 1 \geq 4 + 8$

$15 \geq 12$

1	2	3	4	5	6	7	8	9	10	11	12
1	0	1	1	1	0	0	1	0	0	1	0

- The check bit are in a bit numbers 1, 2, 4, & 8
- Check bit 8 calculated by values in a bit numbers: 9, 10, 11, & 12.
- Check bit 4 calculated by value in bit numbers: 5, 6, 7, & 12
- Check bit 2 calculated by value in bit numbers 3, 6, 7, 10 & 11.
- check bit 1 calculated by value in Bit numbers: 3, 5, 7, 9, 10 & 11

Thus the Check bits are: 1011

part (D)

Part (D)

(18)

Sol

7200 revolution in 60 sec
1 revolution in 60/7200 OR
1 revolution in 6ms
1 revolution = covering one entire track = 500 Sector
500 Sector = 6ms
1 Sector = 8 microsecond.
Now there are 2 different things
(1) 2500 Sectors so time = 2500 × 8ms = 20ms

(2) 1.28 MB = 1342177.28 Bytes OR 2621.44 Sectors = 2622 Sectors = 20.976ms

Total time case:

case (1) 4 + 2 + 20 = 26ms
case (2) 4 + 2 + 20.976 = 26.976ms