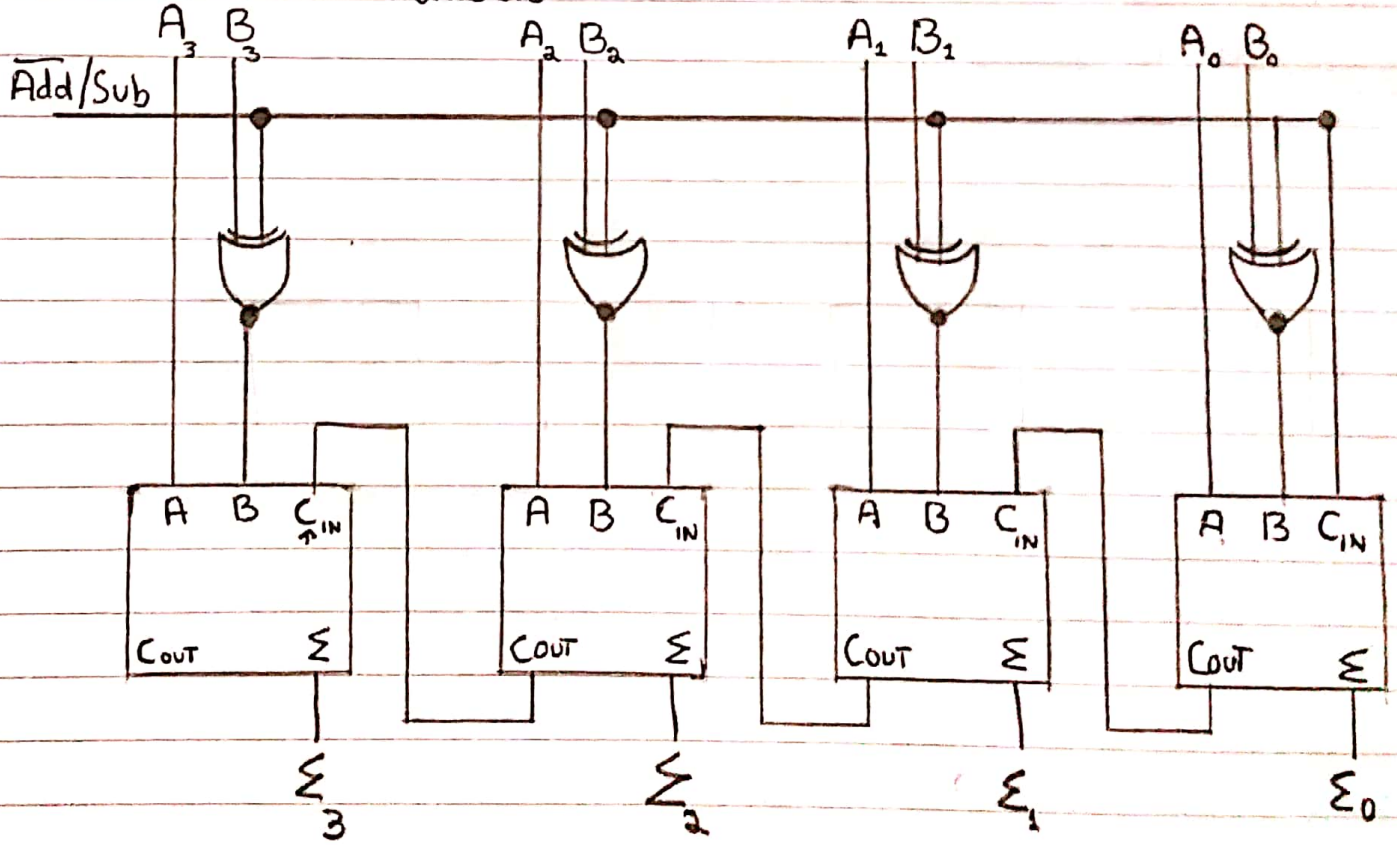
Digital Logic & Design (Final Major Assignment)

Date ID: 12290

Student Name: Aamir Saleem
Student ID : 12290
Session : Summer 2020 major Assignment
Subject : Digital logic & Design
Instructor: Sir Muhammad Amin
Date : 20-9-2020

Q1 Draw & explain the logic diagram for each of the following.

a) A circuit for adding or subtracting 2 4-bit numbers



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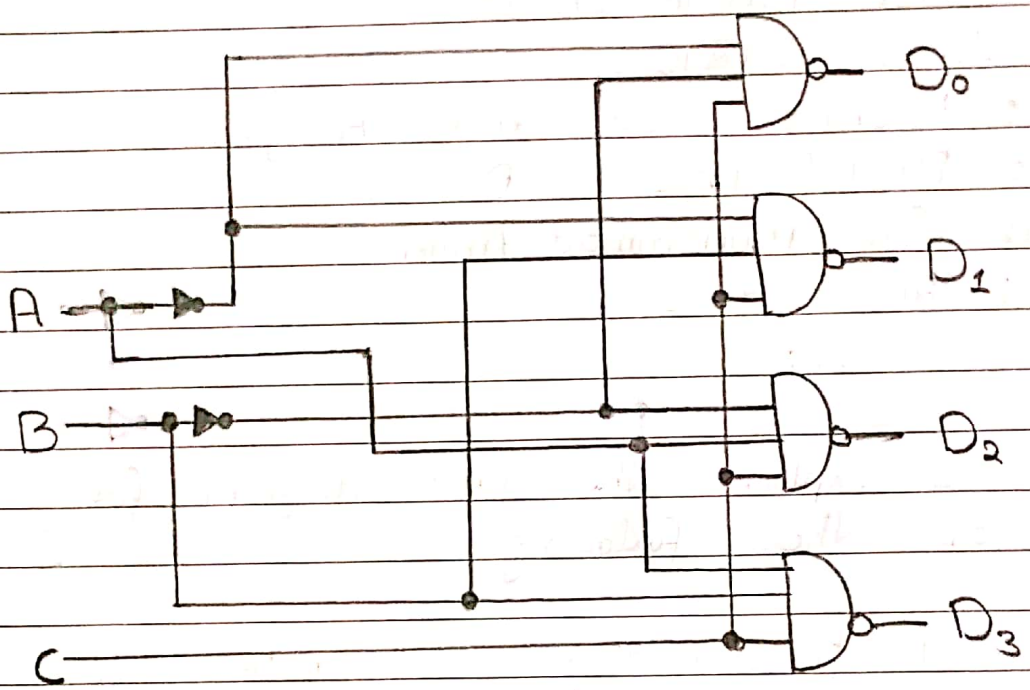
(b) 4- bit active low decoder.

Logic diagram:



Truth table:

C	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

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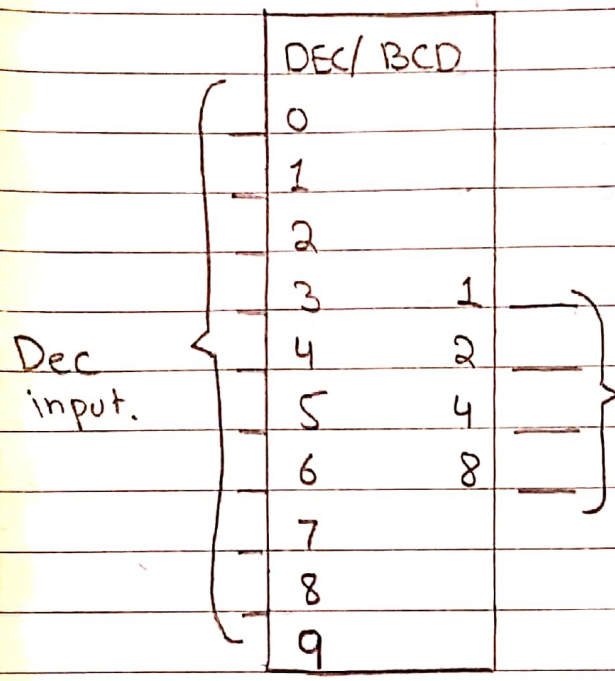
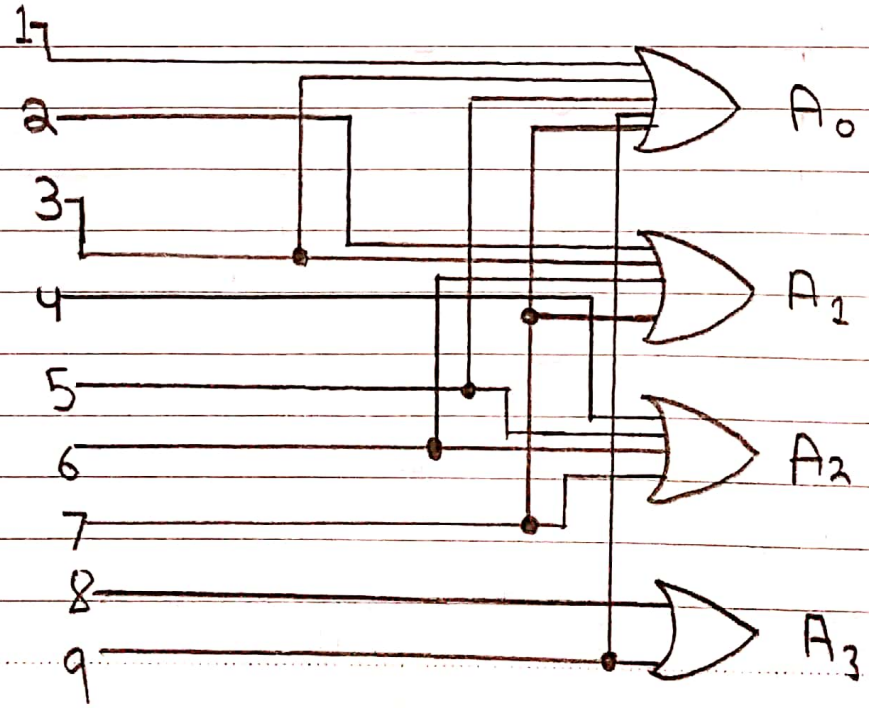
(C) Decimal to BCD ~~converter~~ Encoder.

Ans:- Logic symbol for decimal to BCD encoder:-



Logic Circuit for decimal to BCD encoder:-



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Q2 For the 4-input multiplexer data inputs are given

$D_0 = 0$, $D_1 = 1$, $D_2 = 0$, $D_3 = 1$

Find output Y

a) $S_0 = 1$, $S_1 = 0$ = D_2 = 0

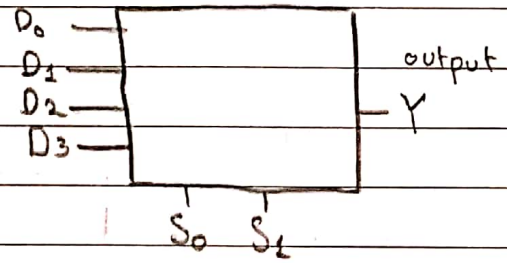
b) $S_0 = 0$, $S_1 = 1$ = D_1 = 1

c) $S_0 = 1$, $S_1 = 1$ = D_3 = 1

d) $S_0 = 0$, $S_1 = 0$ = D_0 = 0

Solution:- We will use 4x1 multiplexer

Block diagram:



Truth table:

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

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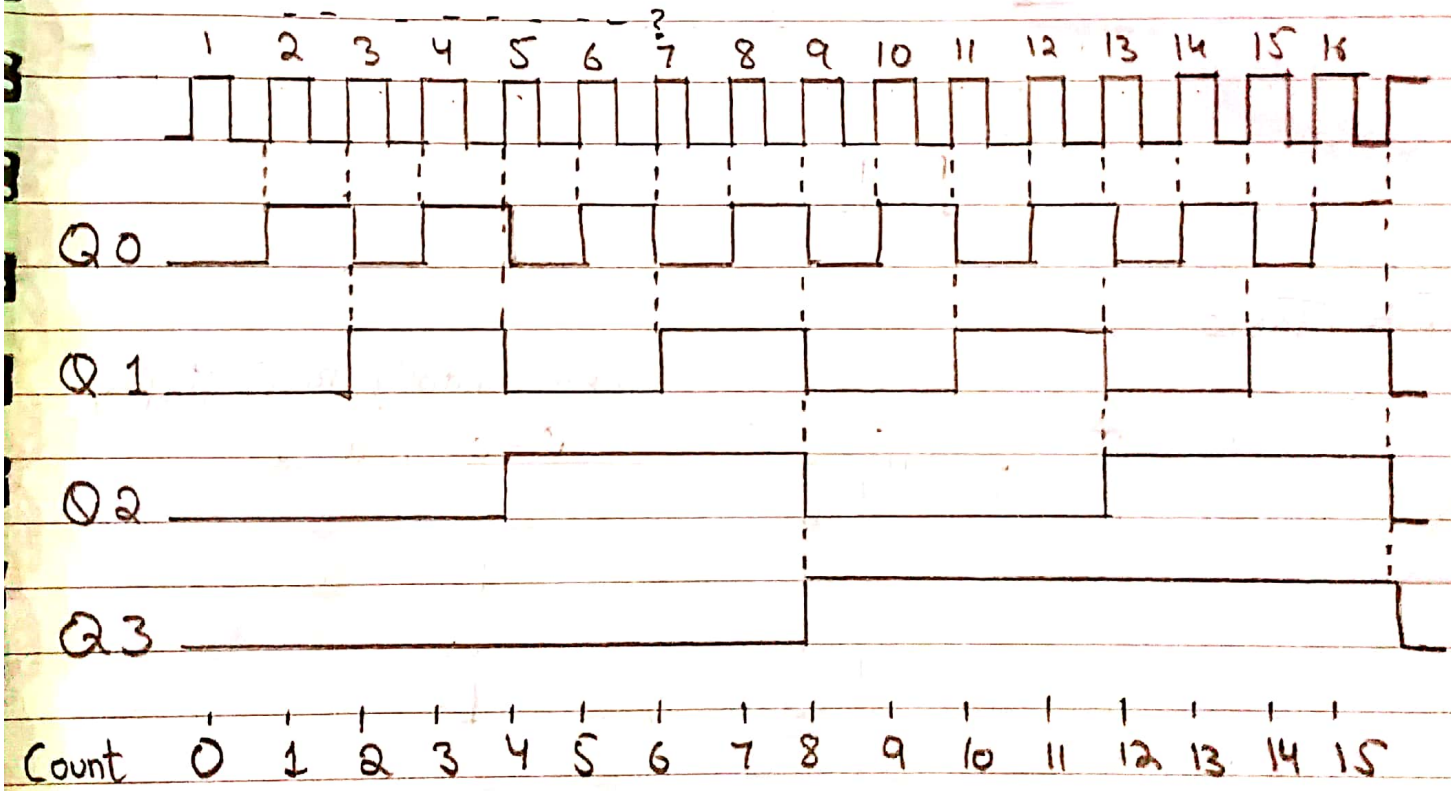
Now putting given value and finding output Y

S_0	S_1	output	Data inputs
$S_0 = 1$	$S_1 = 0$	$Y =$	$D_2 = 0$
$S_0 = 0$	$S_1 = 1$	$Y =$	$D_1 = 1$
$S_0 = 1$	$S_1 = 1$	$Y =$	$D_3 = 1$
$S_0 = 0$	$S_1 = 0$	$Y =$	$D_0 = 0$

Q6: Draw logic & timing diagram for 4- Stage sychornous binary counter. Verify waveform of Q output -



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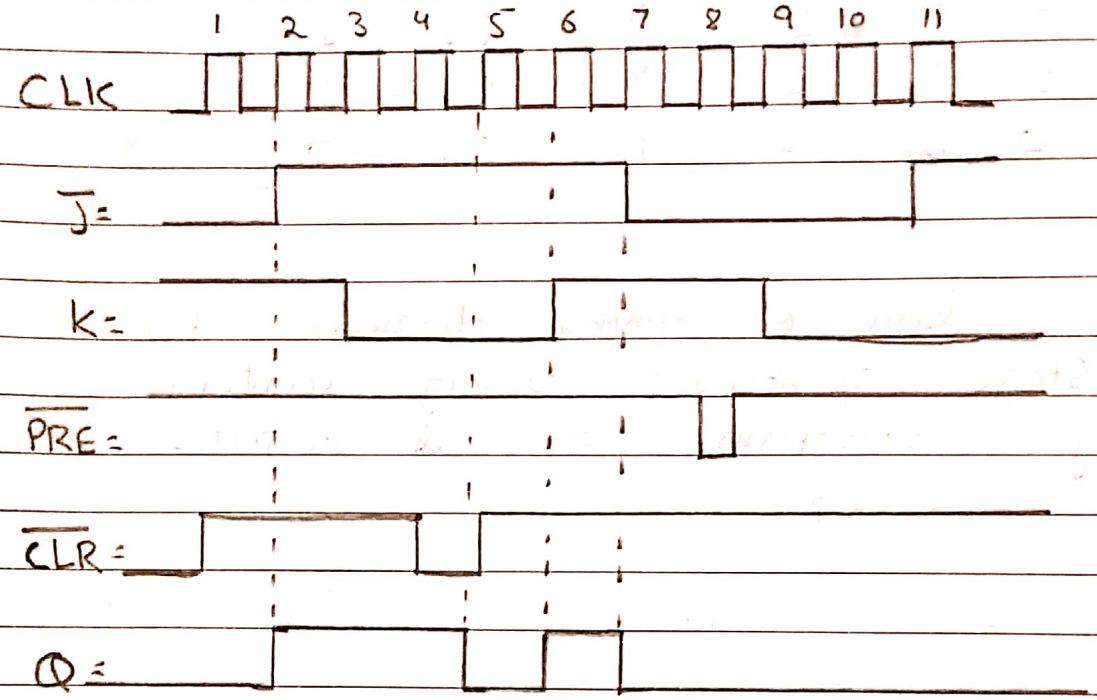
Q4 The waveform in fig 02 are applied to the J, K, CLK, $\overline{PRE}$ & $\overline{CLR}$ input ----------?

Ans:-



Truth Table

Clicks	J	K	$\overline{PRE}$	$\overline{CLR}$	Q
1	0	1	1	1	0
2	1	1	1	1	$\overline{Q}$=1
3	1	0	1	1	1
4	1	0	1	1	1
5	1	0	1	0	0
6	1	1	1	1	$\overline{Q}$=1
7	0	1	1	1	0
8	0	1	0	1	0
9	0	0	1	1	Q=0
10	0	0	1	1	Q=0
11	0	0	1	1	Q=0

When initially RESET flip-flop

Q = 0 , $\overline{Q}$ = 1

J	K	Q
0	0	Q_0
1	0	1
0	1	0
1	1	Toggle

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Q5 Use waveforms in Fig 3 to draw timing diagram for parallel outputs Q_1, Q_2, Q_3, Q_4 ---------?

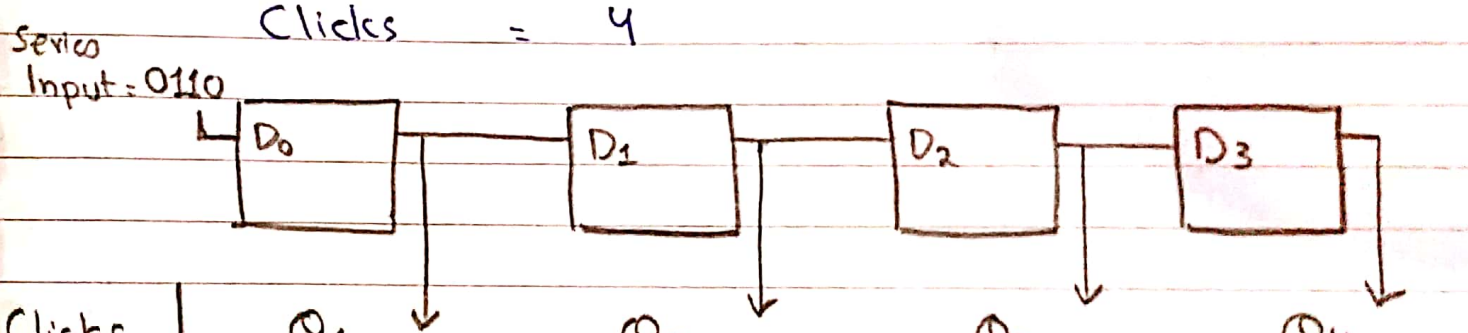
Ans:-

We will use series-in, parallel-out register in this case because we have 1 data input and 4 outputs

Now assuming that register is cleared to 0, 0, 0, 0

Data input = 0, 1, 1, 0

Clicks = 4



Clicks	Q_1	Q_2	Q_3	Q_4
1	0	0	0	0
2	1	0	0	0
3	1	1	0	0
4	0	1	1	0

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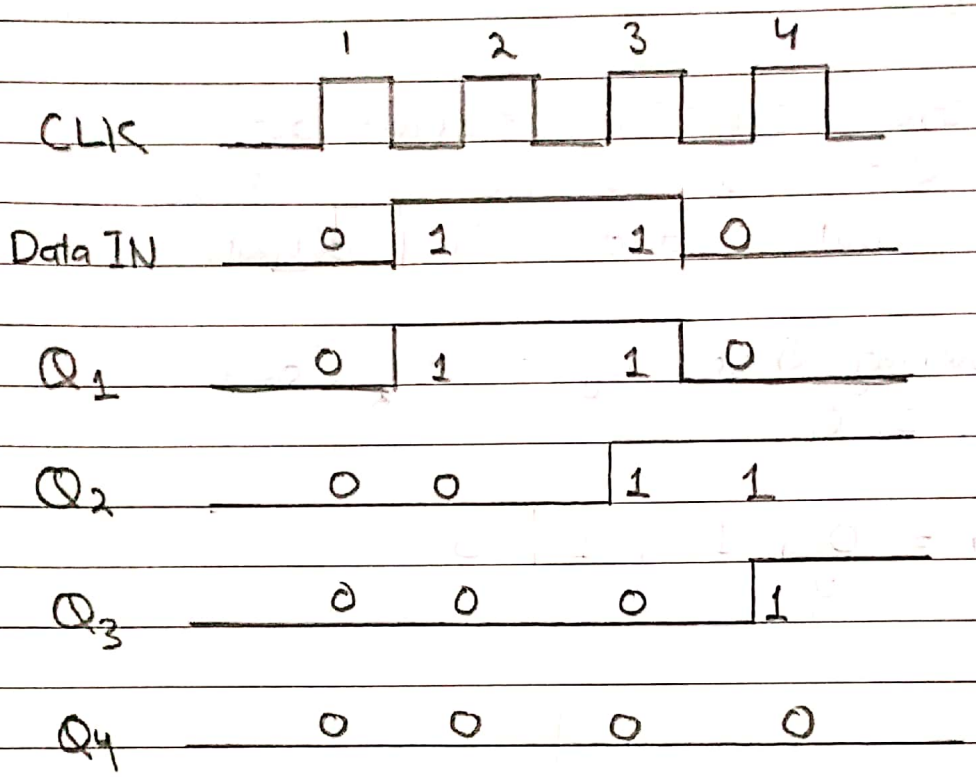
Timing diagram for all outputs.



FINISH.