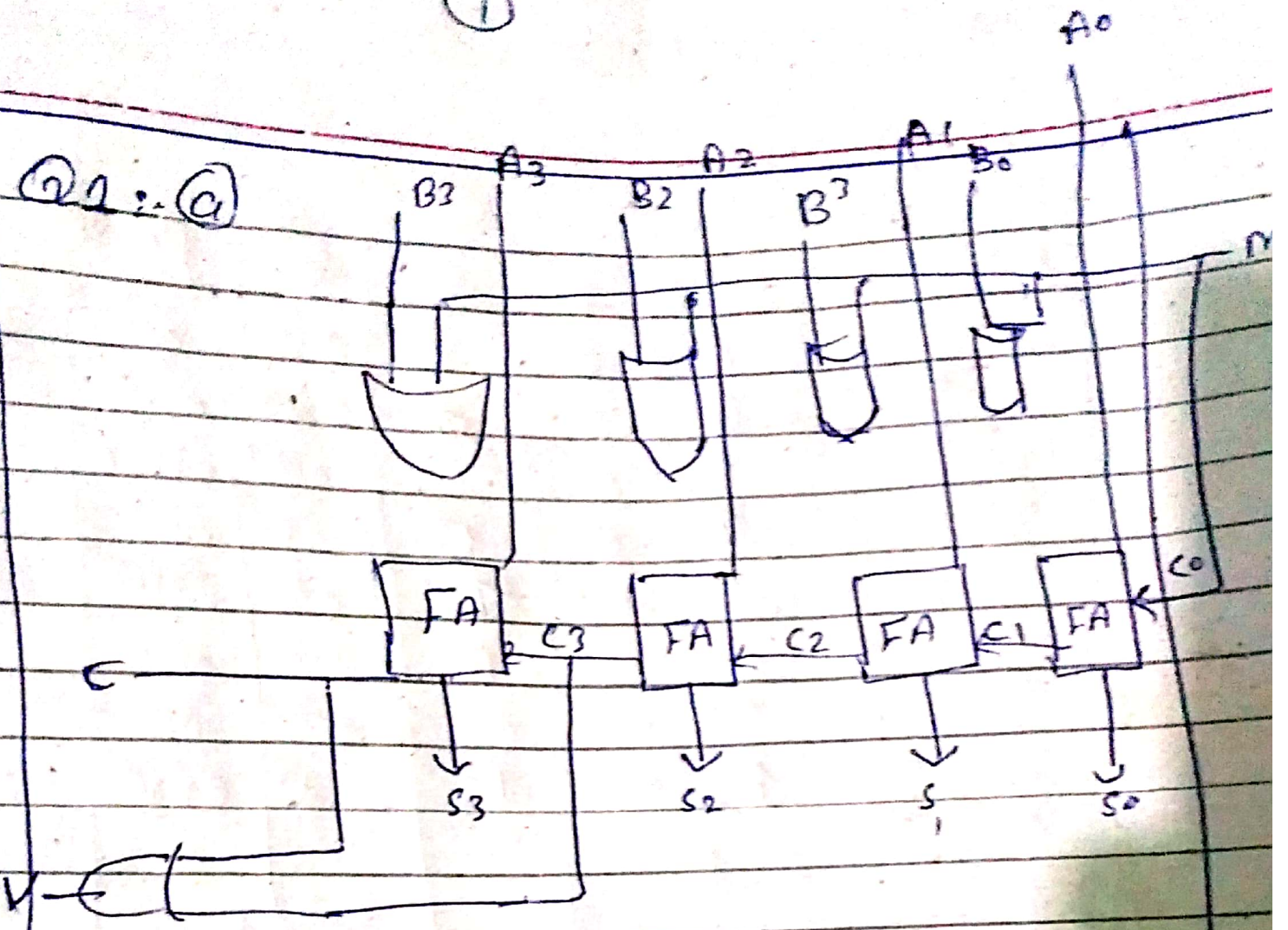
ID 12422

Name Younas Ichan

Subject DLD

Instructor Mohammad Amin

Q1 :- (a)



Q2 :-

Truth table

INPUTS						OUTPUT
B	A	S_0	S_1	S_2	S_3	S
0	0	0	S	S	S	0
0	0	1	S	S	S	1
0	1	S	0	S	S	0
0	1	S	1	S	S	1
1	0	S	S	0	S	0
1	0	S	S	1	S	1
1	1	S	S	S	0	0
1	1	S	S	S	1	1

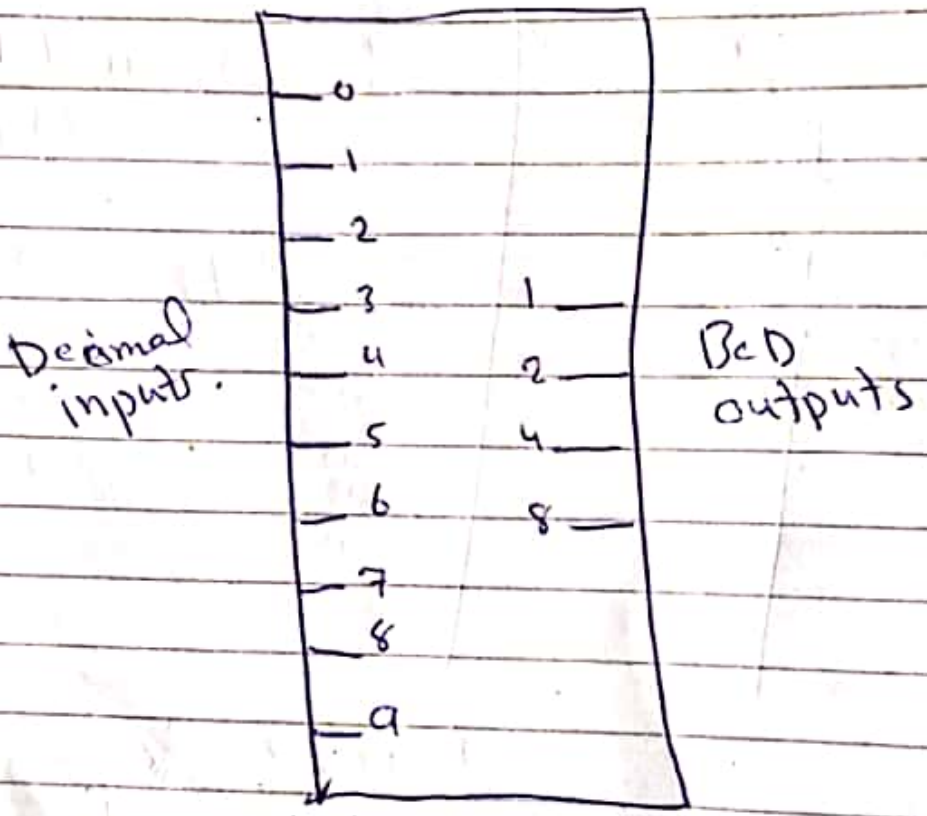
Q1 (B)

if an active low output is required for each decoded number the entire decoder can be implemented with NAND gates and inverters Four Inputs and sixteen outputs.

(C)

Decimal to BCD Encoder

This type of encoder has ten inputs one for each decimal digits and four outputs corresponding to the BCD codes

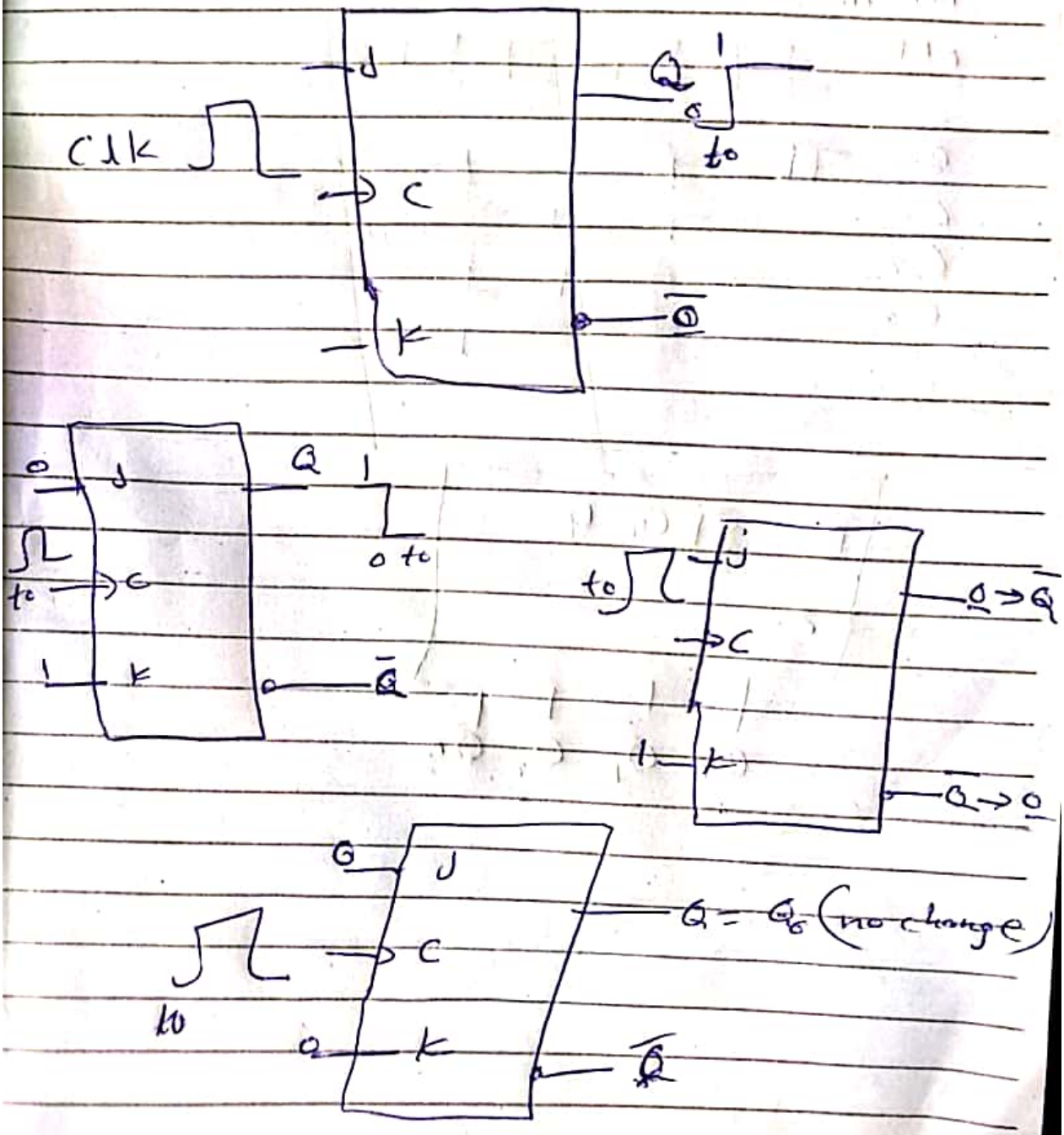


You can determine the relationship between each BCD bit and the decimal digits in order to analyze the logic.

(d)

J-K Flip Flop

The J and K inputs of the J-K flip flops are synchronous inputs because data on these inputs are transfered to the flip flop output only on the triggering edge of the clock pulse.



Q NO3:

Entry	Inputs D1	D2	P	Output C	E	Result
0	0	0	0	0	0, even	ok
1	0	0	0	1	1 odd	error
2	1	0	0	1	1 odd	error
3	1	1	0	0	2 even	ok
4	0	0	1	1	1, odd	error
5	0	1	1	0	2, even	ok
6	1	0	1	0	2, even	ok
7	1	1	1	1	3, odd	error
8						

Ans 4

Solution

Since this is a negative edge-triggered flip-flop, as indicated by the "bubble" at the clock input, the Q output will change only on the negative-going edge of the clock pulse.

1. At the first clock pulse, both J and K are HIGH; and because this is a toggle condition, Q goes HIGH.
2. 2. At clock pulse 2, a no-change condition exists on the inputs, keeping Q at a HIGH level.
3. 3. When clock pulse 3 occurs, J is LOW and K is HIGH, resulting in a RESET condition; Q goes LOW.
4. 4. At clock pulse 4, J is HIGH and K is LOW, resulting in a SET condition; Q goes HIGH.
5. 5. A SET condition still exists on J and K when clock pulse 5 occurs, s remain HIGH.

Ans 5

Counters

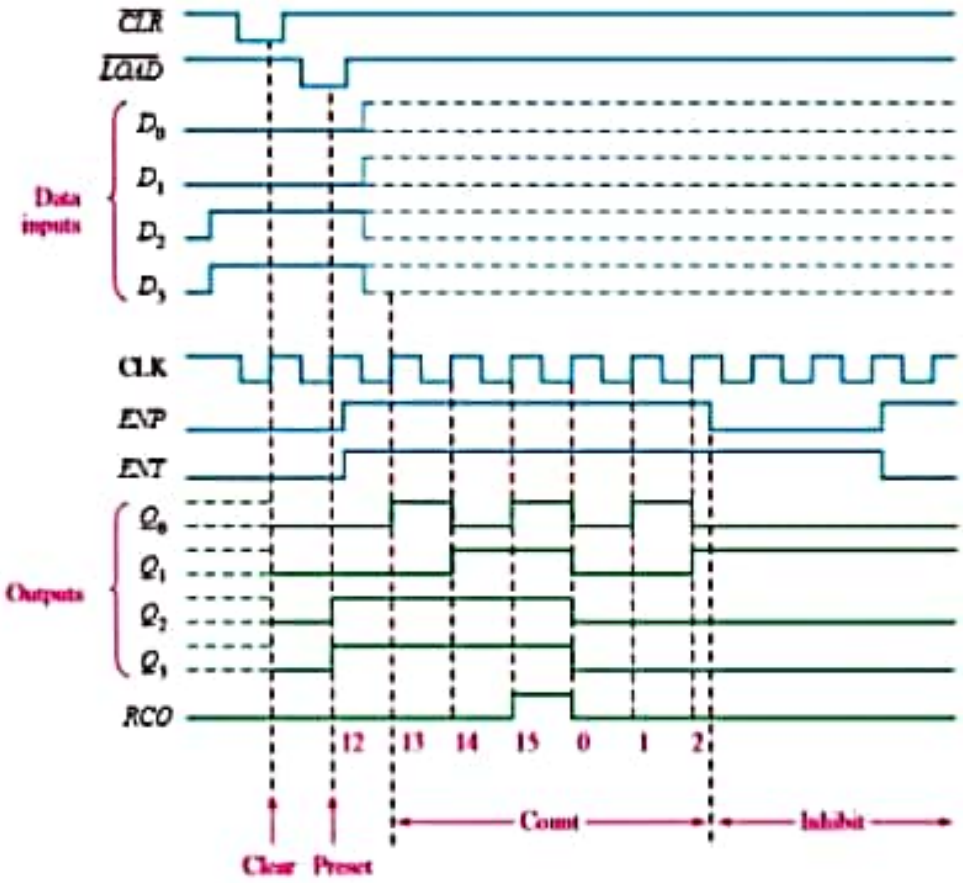


FIGURE 9–21 Timing example for a 74HC163.

Logic diagram

Ans 5

IMPLEMENTATION: 4-BIT SYNCHRONOUS BINARY COUNTER

Fixed-Function Device The 74HC163 is an example of an integrated circuit 4-bit synchronous binary counter. A logic symbol is shown in Figure 9–20 with pin numbers in parentheses. This counter has several features in addition to the basic functions previously discussed for the general synchronous binary counter.

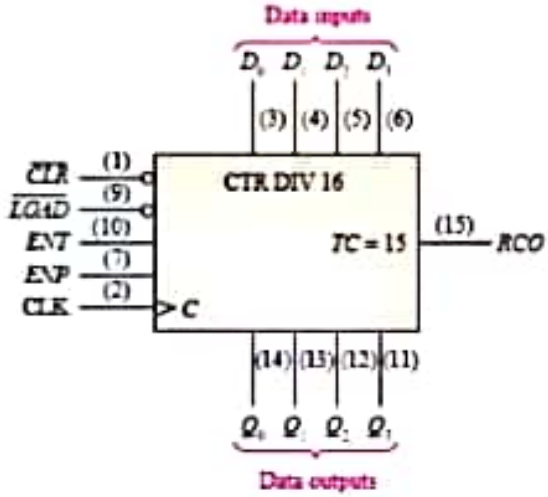


FIGURE 9–20 The 74HC163 4-bit synchronous binary counter. (The qualifying label CTR DIV 16 indicates a counter with sixteen states.)

Ans 5

Counters

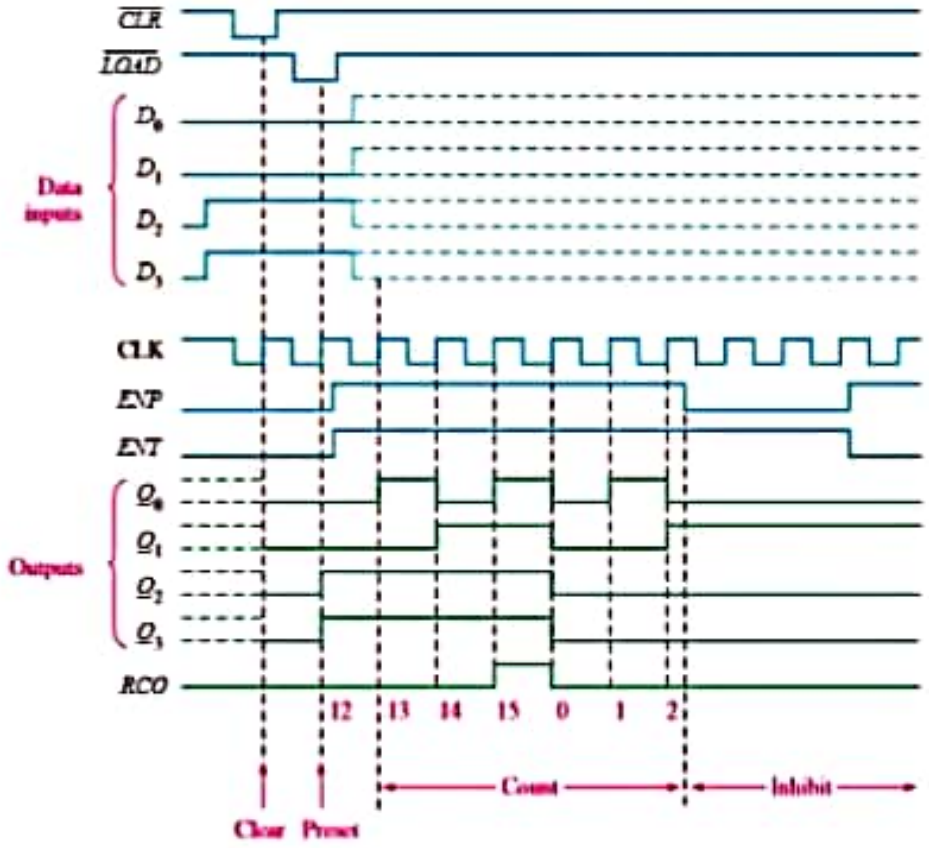
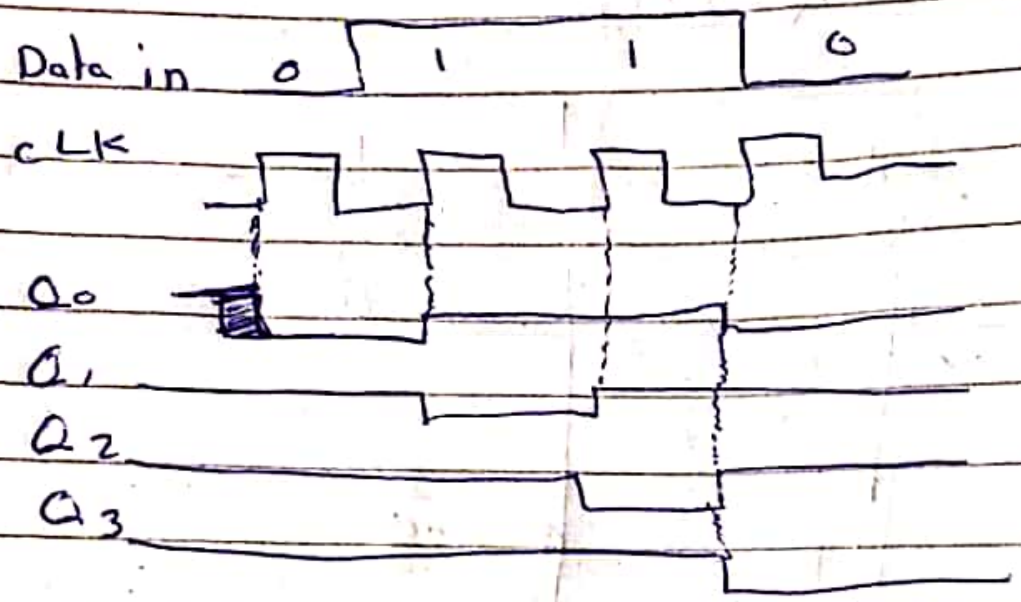
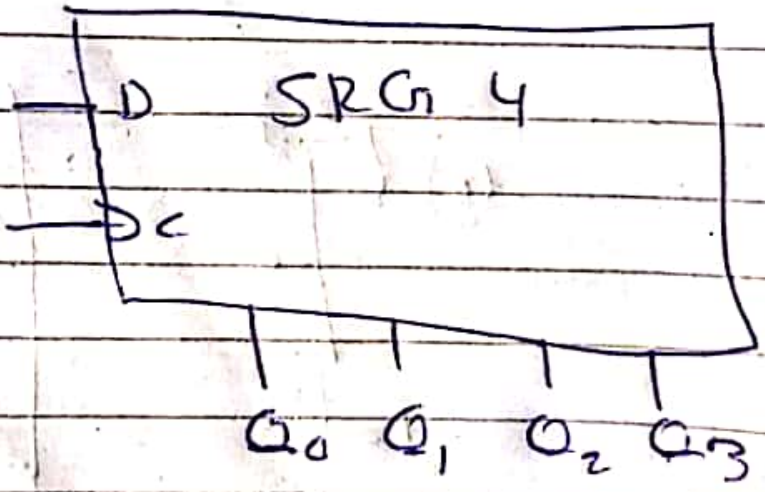


FIGURE 9–21 Timing example for a 74HC163.

Logic diagram

Ans 5





Ans 6

Counters

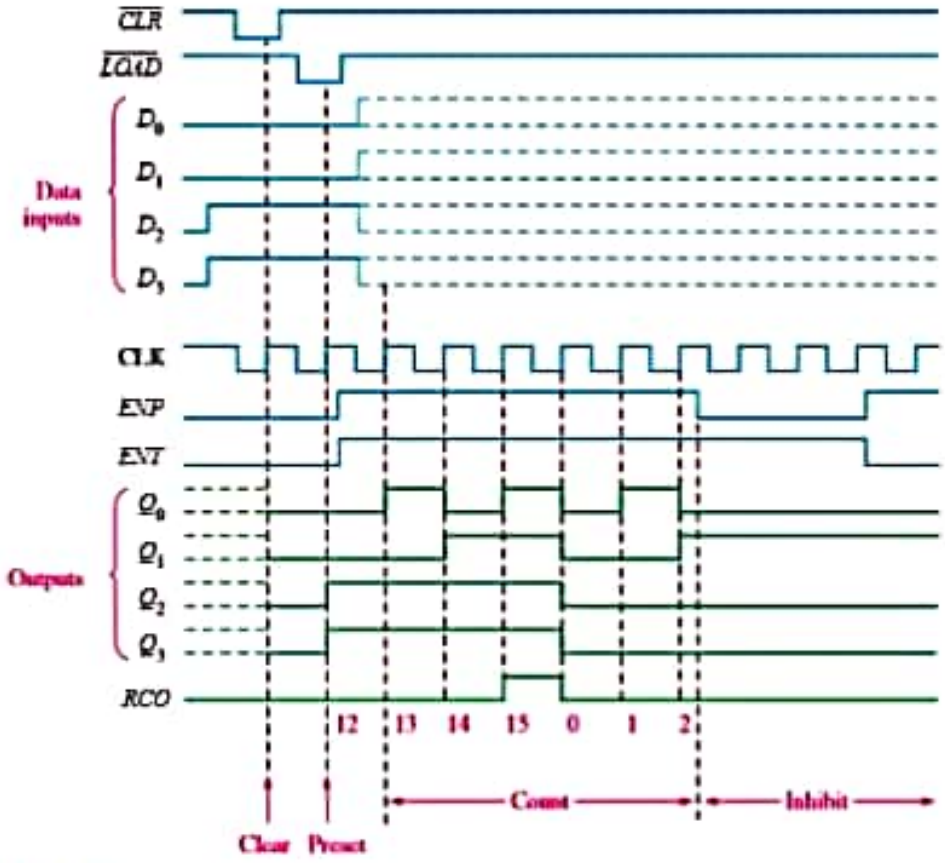


FIGURE 9–21 Timing example for a 74HC163.

Logic diagram

Ans 6. Timing diagram

IMPLEMENTATION: 4-BIT SYNCHRONOUS BINARY COUNTER

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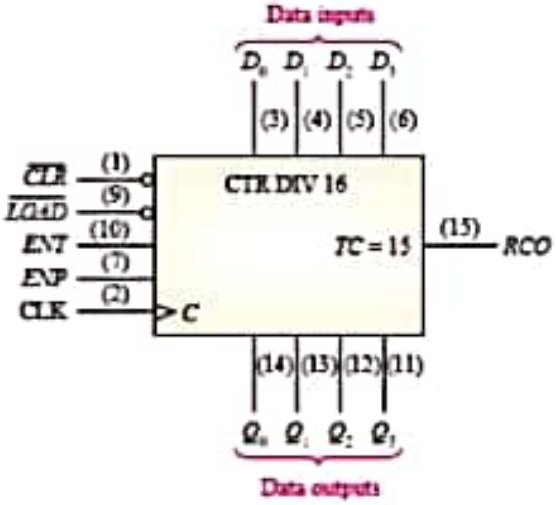

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