Name :: Asad Amin
ID :: 6762
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Q No 1

(a)

Ans The given below are there some of the techniques used to increase the speed are:

(1) Pipelining :-
Pipelining enable to processor to work simultaneously on multiple instructions by performing a differerent phase for each of multiple instructions.

(2) Branch prediction :-
Branch prediction patentially increase the amount of work available for the processor to execute.

(3) Super scalar execution :- This is the ability to issue more then one instruction in every processor clock cycle.

(b)

Ans The speedup using a parallel processor with N processors that fully exploits the parallel position of the program is as follows:

Speed up = Time to execute a program on a single processor / Time to execute program on N-parallel processor

$= T(1-f) + Tf / T(1-f) + Tf/N =$

$1 / (1-f)$

(c)

Ans QPI Layer:- In this layer the packet is defined as the unit of tranfer one key function performed at this level is a cache coherency protokal, which deals with making sure that main memory values held in multiple cache are consistant. A typical data packets pay load is a block of data being send to or from a cache.

(d)

Ans A root complex device also referred to as a chipset or a host bridge connects the processors and memory sub systems to the PCI express switch fabric comprising one or more PCIe and PCI switch device.

PCIe links from the chipset may attached to a following devices.

(1) Switch:- The switch manages multiple PCIe streams.

(2) PCIe end point:- As I/o devices or controller that implement PCIe such as Giga bit ethernet switch disk interface or communication controller etc.

(3) PCI or PCIe bridge:- Allows PCI older devices to be connected to PCIe based system.

Q No 2

(a)

Ans Gorden Moore observed that the number of transistors was doubling every year on a single chip pace slowed to a doubling every 18 months in the

1970's but has substained that rate since

(1) The cost of computer.
(2) The electrical path length is shortened increasing operating
(3) The computer becomes smaller.

(b)

Ans

Similar or identical instruction set:- This mean that program can move up but not down.

Identical operating system :- The same basic os is available for all family members.

Increases memory sizes :- Increasing the main memory size is going to family.

Increasing cost :- Its also sent from lower to higher family member.

(c)

Ans Instruction fetch :- Read instruction from its memory location into the processor.

Instruction operation decoding (IOD):- Analyse instruction to determine type of operation to be performed and operands to be used.

Operand fetch:- Fetch the operand from memory or read it in form I/O.

Operand store:- Write the result into memory or out to I/O.

(d)

Ans Program:- It is generated by some condition that occurs as a result of an instruction execution, such as arithmatic overflow division by zero, or reference outside a users allowed memory spaces.

Hardware failure:- It is generated by a failure such as power failure or memory parity error.

Timer:- It is generated by a timer within the processor. This allow the operating system to perform certain functions on a regular basis.

I/O:- It is generated by I/O controller

to signal normal completion of an operation request service from the processor.

QNo3

(a)

Ans Cortex A :-

The cortex A and cortex A 50 are application processor intended for mobile devices such as smart phones and E-book readers, digital TV home gateway etc.

Cortex-R :-

The cortex R is designed to support real time application in which the time of event need to be controlled with rapid respond to events. They run at a high frequency e.g 200 MHz to 800 MHz.

Cortex-M :-

Cortex-M series processors have been developed primary for the Microcontroller domain where the need for fast highly deterministic interrupt. Mangement is coupled with the desire for extremely possible power consumptions.

(b)

Multicore :-

The use of multicore processor

This is the control logic the traffic through the

on the same chip provides the potential to increase performance without increasing the clock ratio.

MIC:

Leap in performance as well as the challenges in developing software to exploit such as a large number of core.

GpGpu:-

GPGPU core designed to perform parallel operations on graphic data it is used to encode and render 2D and 3D graphics.

(c)

Ans) Disabled Interrupt:-

Simply mean that the processor can and will ignore that interrupt request signal

Nested Interrupt:-

It is to allow an interrupt of higher priority to cause a lower priority interrupt handler to be itself interrupted.

QNo 5

Ans

Find CPI, Mips Rate and execution time for this program.

$$CPI = \frac{(1 \times 46000) + (2 \times 33000) + (2 \times 16000) + (2 \times 9000)}{100}$$

$$CPI = \frac{46000 + 66000 + 32000 + 18000}{100}$$

$$CPI = \frac{162000}{100} = 1620$$

CPI = 1620 Ans.

Mips Rate I = 104000

Mips Rate = 60 MHz / 1620 × 10^6

= 60 × 10^6 / 1620 × 10^6

Mips Rate = 0.037 Ans

Execution time

T_e = I_c / (Mips Rate × 10^6)

T = 104000 / (0.037 × 10^6)

T = 104000 / (37 × 10^3)

T = 104000 / 37000

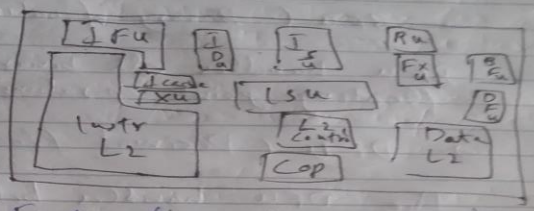
T = 104 / 37

T = 2.811

Ans

Q No 4

(a)



→ IDU (Instruction decode unit) :- The IDU is responsible for the parsing and decoding of all Z/Architecture operation codes.

→ LSU (Load Store unit) :- It is responsible for handling all type of operands access of all lengths, modes and formats.

→ XU (Translation Unit) :- This unit translate logical address from instruction into physical addresses in the main memory.

→ FXU (Fixed point unit) :- The FXU

execute fixed point arithmatic operations.

→ BFU (Binary floating point Unit) :-
The BFU handles all binary and hexadecimal floating point operations.

→ DFU (Decimal floating point unit) :-
The DFU handles both fixed point and floating point operations on numbers that are stored as decimal digits.

→ RU (Recovery Units) :-
The RU keeps a copy of complete state of the system that include all registors.

→ COP (Dedicated Co-processor) :-
The COP is responsible for data compresion and encryption function for each case.

→ I cache :-
This is the 64 kb L1 instruction cache allowing the IFU to prefetch instruction before they are needed

→ L2 cache :-
This is the control logic that manages the traffic through the

Power

(c)

Instruction fetch :-

two L2 cache.

→ Data L2 :-
1 MB L2 cache for all memory traffic other than instruction

→ Instr L2 :-
1 Mb instruction cache

(b)

IAS instructions or operations :-

(1) data transfer - Move data between MEM & ALU or two ALU's registers
(2) Unconditional branch - branch to some location unconditionally execution may not be sequential in this case.
(3) Arithmatic - ALU operations.
(4) Address modify - Addresses in the an instruction can be modified.