Department of Electrical Engineering
Mid-term
Date: 24/08/2020

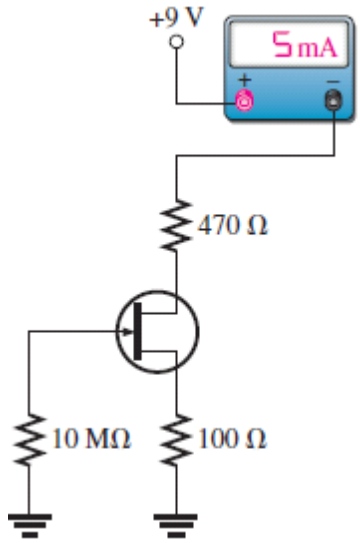
Course Details

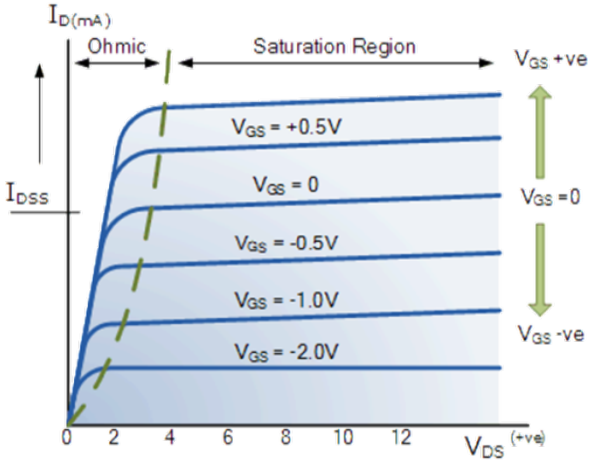
Course Title: Electronic Circuit Design **Module:** 6th
Instructor: Dr Sheharyar **Total Marks:** 30

Student Details

Name: **Talha Khan** **Student ID:** **13845**

Student Signature: _____

Q1.		For the circuit given in figure 1. Answer the following: a) Which type of transistor is that? b) Label the Drain, Source and Gate. c) Determine the values of V_{DS} and V_{GS}  **Figure 1**	Marks 09
Q2.		**Explain** the drain characteristic curve of D-MOSFET given below in Fig. 2.	Marks 06

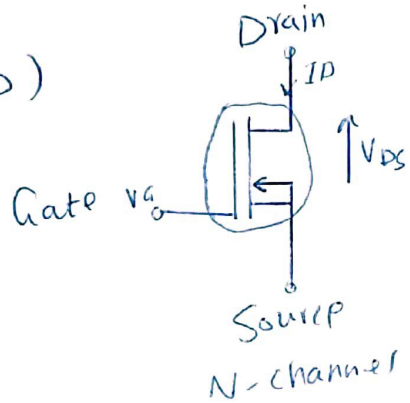
		 **Figure 2**	
Q3.		**Sketch** the hybrid equivalent for common emitter transistor. Write equations for the transistor in common emitter configuration.	Marks 05
Q4.		**Explain** why both types of MOSFETs have an extremely high input resistance at the gate. (Marks 01) In **what** mode an *n*-channel D-MOSFET with a positive *V*GS is operating? (Marks 01) **Why** must the gate-to-source voltage of an *n*-channel JFET always be either 0 or negative? (Marks 01) **Briefly discuss** that how BJT differs from FET? (Marks 04) MOSFET is also called IGFET, give reason **why**? (Marks 01) **Why** JFET is called Squared Law Device? (Marks 01) **What** can be the main disadvantage of common-base amplifier as compared to the common-emitter and emitter-follower amplifiers? (Marks 01)	Marks 10

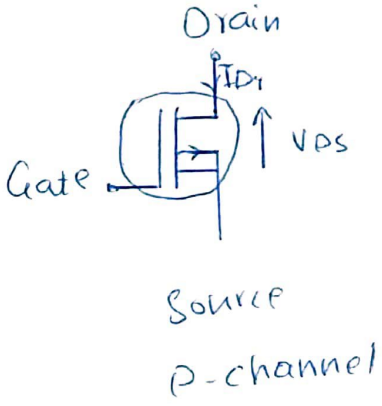
Q(1)

Ans:-

(a) This is a PNP Transistor.

(b)





(c) $V_S = (5\,mA)(100\,\Omega) =$

$0.5\,V$

$V_D = 9V - (5mA)(470\Omega)$

$= 6.65V$

$V_G = 0V$

$V_{GS} = V_G - V_S$

$= 0V - 0.5V$

$= -0.5V$

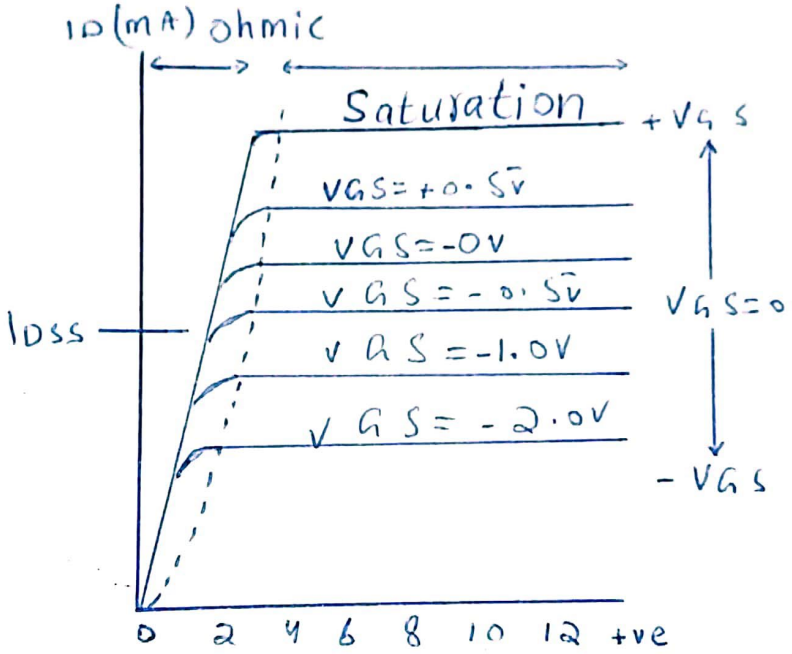
$V_{DS} = V_D - V_S$

$V_{DS} = 6.65V - 0.5V$

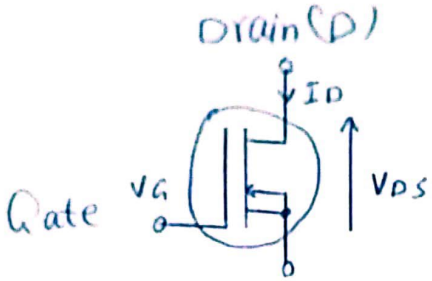
$V_{DS} = 6.15V$

Q(2)

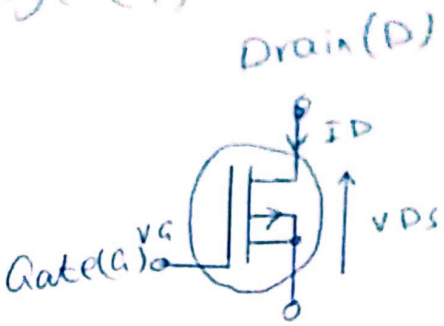
Ans:-



Characteristic Curve of Depletion Mode MOSFET



N-Channel



P-channel

This characteristic mainly gives the relationship between drain-source voltage (V_{DS}) and drain current (I_D).

The small voltage at the gate controls the current flow through the channel.

The channel between drain and source acts as a good conductor with zero bias voltage at gate terminal.

The channel width and drain current increases if the gate voltage is positive and these two (channel width and drain current) decreases if the gate voltage is negative.

Cut-off Region:-

If the gate-source voltage is less than the threshold voltage then we say that the transistor is operating in the cut-off region. (i.e fully OFF). In this region drain current is zero and the transistor acts as an open circuit.

$$V_{GS} < V_{TH} \Rightarrow I_{DS} = 0$$

Saturation Region:-

In this region the gate voltage is much greater than threshold voltage and the drain current at its maximum value and the transistor is in fully (ON) state.
In this region the transistor acts as a closed circuit.

$V_{GS} >> V_{TH}$ and $(V_{GS} - V_{TH}) < V_{DS} < 2(V_{GS} - V_{TH})$

$\Rightarrow I_{DS}$ = Maximum

The gate voltage at which the transistor (ON) and starts the current flow through the channel is called threshold voltage.

Ohmic Region:-

If the gate is greater than threshold voltage and the drain-source voltage lies between V_{TH} and $(V_{GS} - V_{TH})$ then we say that the transistor is in linear region and at the state the transistor acts as a variable resistor.

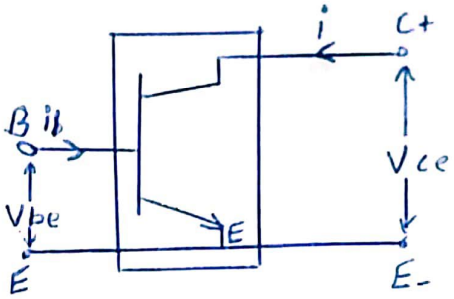
$V_{GS} > V_{TH}$ and $V_{TH} < V_{DS} < (V_{GS} - V_{TH})$ $\Rightarrow$ MOSFET acts as a variable resistor.

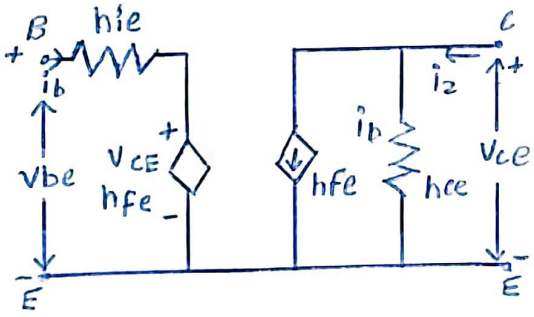
This threshold voltage value range for N-Channel devices is in between 0.5V to 0.7V and for P-channel devices is in between -0.5V to -0.8V.
The behavior of a MOSFET transistor in depletion and enhancement modes depending on the gate voltage is summarized as follows.

MOSFET TYPE	V_{GS} = +VE	V_{GS} = 0	V_{GS} = -VE
(1) N-Channel Depletion	ON	ON	OFF
(2) N-Channel Enhancement	ON	OFF	OFF
(3) P-Channel Depletion	OFF	ON	ON
(4) P-Channel Enhancement	OFF	OFF	ON

Q(3)

Ans:-





In common emitter transistor configuration the input signal is applied b/w the base and emitter terminals of the

transistor and output appears between the collector and emitter terminals. The input voltage (V_{be}) and the output current (i_c) are given by the following eq.

$$V_{be} = h_{ie} \cdot i_b + h_{re} \cdot V_c$$

$$i_e = h_{fe} \cdot i_b + h_{oe} \cdot V_c$$

Current Gain:

It is given by the relation

$$A_i = -(h_{fe}/(1 + h_{oe} \cdot r_L))$$

where r_L is the A.C load resistor. Its value is equal to the parallel combination of Resistance R_c and R_L.

Since h_{fe} of a transistor is a positive number, therefore A_i of a common emitter amplifier is negative

Input Resistance:

The resistance looking into the amplifier input terminals (i.e base of a transistor) is given by the relation.

$$R_i = h_{ie} + h_{re} \cdot A_i \cdot r_L = h_{ie} - ((h_{re} \cdot h_{fe}) / (h_{oe} + (1/r_L)))$$

The input resistance of the amplifier stage (called stage input resistance R_{is}) depends upon the biasing arrangement For a fixed bias circuit, the stage input resistance is,

$$R_{is} = R_i // R_B$$

If the circuit has no biasing resistances then $R_{is} = R_i$.

Voltage Gain:

It is given by the relation,

$$A_v = A_i \cdot r_1 / R_i$$

Since the current gain(A_i) of a common emitter amplifier is negative, therefore the voltage gain(A_v) is also negative. It means that there is a phase difference of 180° b/w the input and output. In other words, the input signal is inverted at the output fo a common emitter amplifier. The voltage gain, in terms of h-parameters, is given by the relation.

$$A_v = h_{fe} \cdot r_1 / (h_{ie} + \Delta h \cdot r_L)$$

where

$$\Delta h = h_{ie} \cdot h_{oe} - h_{re} \cdot h_{fe}$$

Output Resistance:

The resistance looking into the amplifier output terminals is given by the relation,

$$R_o = (R_s + h_{ie}) / (R_s \cdot h_{oe} + \Delta h)$$

where

R_s = Resistance of the source, and

$\Delta h = h_{ie} \cdot h_{oe} - h_{re} \cdot h_{fe}$

The output resistance of the stage,

$$R_{oe} = R_o // r_L$$

~~The output resistance~~

Overall voltage Gain:

$$A_v = (A_v \cdot R_{is}) / (R_s + R_{is})$$

Overall Current Gain:

$$A_{ie} = A_j \cdot R_s / (R_s + R_{js})$$

Q 4

Explain why both type of MOSFETs have an extremely high input resistance at the gate.

Ans:-

Gate rests on a thin oxide layer over the source-drain channel. The oxide layer, effectively a dielectric, acts as a capacitor and isolates gate and rest of the substrate body, source, drain and channel. Hence no connection exists between gate and rest of the parts, which means input impedance of a MOSFET is very high.

Q(4)

In what mode an n-channel D-MOS-FET with a positive VGS is ~~open~~ operating?

Ans:- The enhancement-mode.

Q(4) Why must the gate-to-source voltage of an n-channel JFET always be either 0 or negative?

Ans:- The gate-to-source voltage of an n-channel JFET must be zero or negative in order to maintain the required reverse bias condition.

Q(4) Briefly discuss that how BJT differs from FET?

Ans:-

BJT and FET are two different kinds of transistor and also known as active semiconductor devices.

BJT is a Bipolar Junction transistor and FET is a Field Effect transistor.

The major difference between BJT and FET is that, in a field effect transistor only majority charge carries flows, whereas in BJT both majority and minority charge carriers flows.

Q(4) MOSFET is also called IGFET, give reason why?

Ans:- The Insulated-Gate Field-Effect Transistor (IGFET), also known as the metal oxide Field Effect Transistor (MOSFET), is a derivative of the field effect transistor (FET). Today, most transistors are of the MOSFET type as components of digital integral circuits.

Qu: Why JFET is called square law device?

Ans:-

(1) The input-output transfer Characteristic of the JFET is not as straight forward as it is for the BJT.

(2) In a BJT, β (h_{FE}) define the relationship between I_B (input current) and I_c (output current).

(3) In a JFET, the relationship b/w V_{GS} (input voltage) and I_D (output current) is used to define the transfer.

(4) As a result, FET's are referred to a square law devices.

Q(4)

(7) Ans:- In the common base amplifier configuration the input current exceeds all other current, including the output current, the current gain of this amplifier is actually less than 1.