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Dept Bscs

(1)

Give detail answer to each of the following -

a) Discuss different types of semiconductor memories in detail.

ns There are varies types of semi conductor memories

⇒ The Most Common is referred to as RAM (random access memory). Most types have the property of Random Access Memory which means that it takes the same amount of time to access any memory location.

Here is the table of Semi Conductor Memory types

Memory type	Category	Elasule	write mechanism	Volatility
RAM (random memory)	Read/write memory	Electricity Bite level	Electrically	Volatile
ROM	Read only Memory	Not Possible	Masks	Non Volatile
PROM				
EPROM		UV light chip level		
FERROM	Read mostly Memory	Electrically Byte level	Electrically	
Flash memory.		Electrically block level		

b Explain the read write operation for the SRAM cell Using diagram

Ans

Read Operation:-

In SRAM, for only operation. to be performed, the word line Shoud be high. To perform read operation, initially.

Write Operation:-

Consider the memory bits Consists of Q = 0 and Q' = 1.

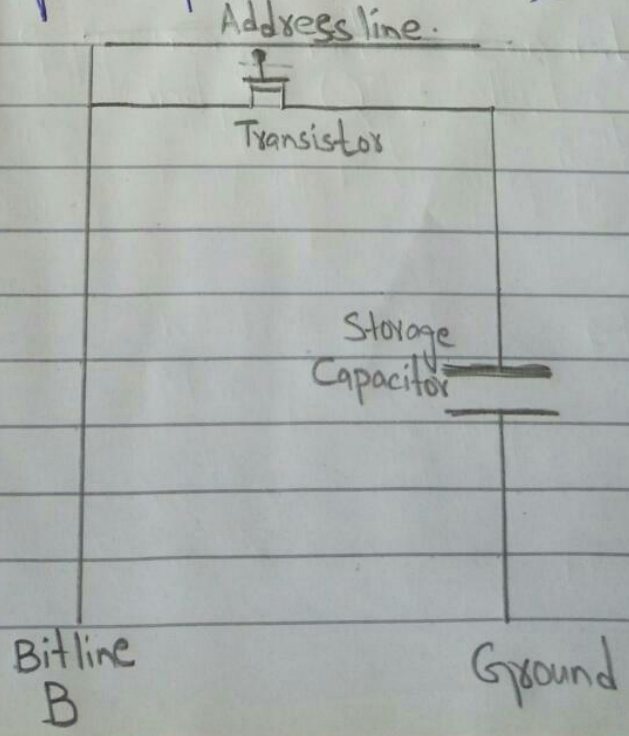
C Explain the read and write operation for the DRAM cell using diagram.

Ans **Read operation:-**

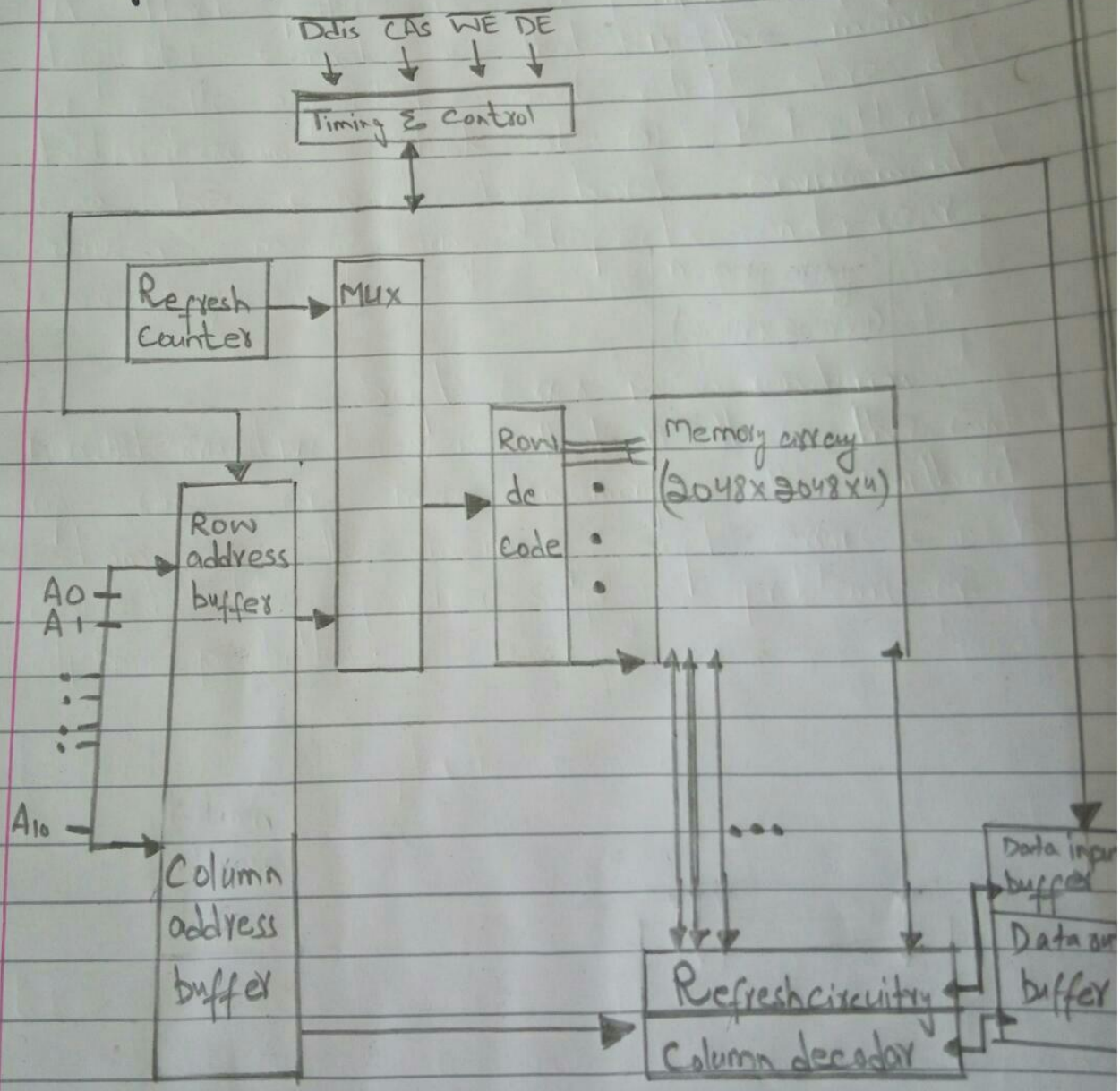
When the address line is selected, the transistor turns on and the charge stored on the capacitor is fed out into a bit line & to a sense amplifier. it compares the capacitor voltage to a reference value & determines if the cell contains a logic 1 or a logic 0.

Write operation:-

A voltage signal is applied to a bit line. a high voltage represents 1 & a low represent 0.



d) Discuss 16_Mbit DRAM (4M×4) organization using diagram



Typical 16_Mbit DRAM (4M×4)

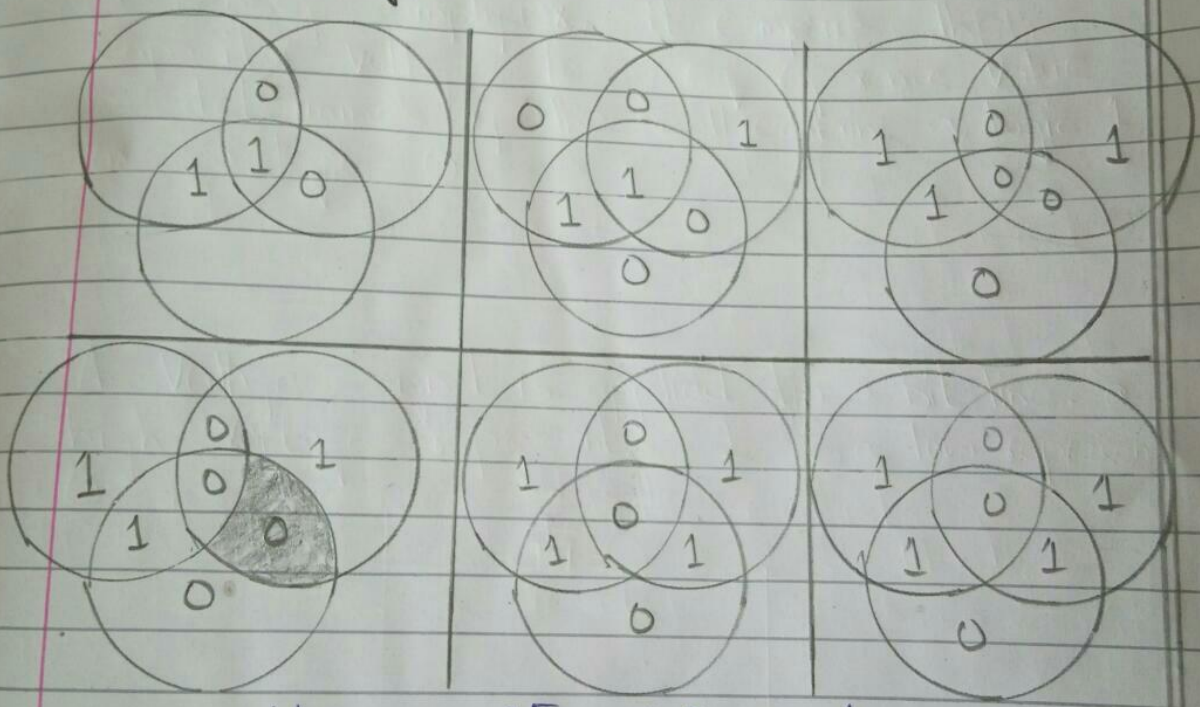
Because only 4 bits are read/written to this DRAM, there must be multiple DRAMs connected to the memory controller to read/write a word of data to the bus.

All the DRAMS require a refresh operation. A simple technique for refreshing is in effect, to disable the DRAM chip while all data cells are refreshed The refresh counter steps through all of the row values. The causes each cell in row to be refresh.

e) Discuss 1MB (256K x 4 x 8Bit) memory organization using diagram.

The possible organization is of a memory consisting of 1M word by 8 bits per word In this case we have four columns of Chips, each column containing 256K words arranged.

f) Explain Hamming SEC-DEC Code Using Venn diagrams.



Hamming SEC-DEC code.

With 1 bit per-chip organization, an SEC-DEC code is generally considered adequate e.g the IBM 30xx implementations Used an 8-bit SEC-DEC Code for each 64 bits of data in main memory. The Size of

main memory is actually about 12% larger than is apparent to the user. The Vax computer used a 7-bit SEC-DEC for each 32 bits of memory, for a 22% overhead.

g) How is Syndrome for the Haming Code interpreted?

Answer Sydrome for Hamming code interpreted as follows.

→ If Syndrome Contain all 0s, no error has been detected.

→ If Syndrome Contain one and only one bit set to 1, than an error has accured in one of the 4 check bit No Correction is needed.

→ If Syndrome Contain more than 1 bit set to 1, then the numerical Value of the Syndrome indicates the position of the data bit in error. The data bit is inverted for Correction

Q2 Differentiate each of the following-

a) DRAM and SRAM.

DRAM	SRAM.
→ Dram is more dense and less expensive	SRAM is expensive
→ DRAM required the supporting refresh circuitry	SRAM doesnot required any refresh circuitry
→ DRAM are normal in Speed	SRAM are faster in speed the DRAM.
→ DRAM is used for main memory	SRAM is used for cache memory

EEPROM and flash memory

EEPROM	Flash Memory.
→ EEROM devices can erase any byte of memory at anytime	Flash Memory can only erase an entire chunk, or sector of memory at tim
→ EEPROM Uses Nor type memory	Flash memory Uses NAND type Memory.
→ EEPROM is bytewise erasable	Flash is block wise erasable.

c) Hard failure and Soft error in Semiconductor memories.

Ans. A Hard failure is a permanent physical defect ~~cannot~~ so that is the memory cell or cells affected cannot reliably store data but became stunk at 0 and 1°. Hard error can be caused by harsh environmental abuse, manufacturing defects and wear.

Where as

Soft error is a random, non-destructive even that alters the contents of one or more memory cells without damaging the memory. Soft errors can be caused by power supply problems or alpha particles.