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Final Paper: DLD

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Note:- Attempt all questions. (3)

Q1 Draw the logic circuit using the input (A, B, C, D) and output (X) waveform in figure.

Ans Solution:

The output expressions wave form X for the circuit is developed in figure 5.35. The SOP form indicates that the output is HIGH when A is low and C is high when B is Low and C is High or when C is Low and D is High.

P.T.O.

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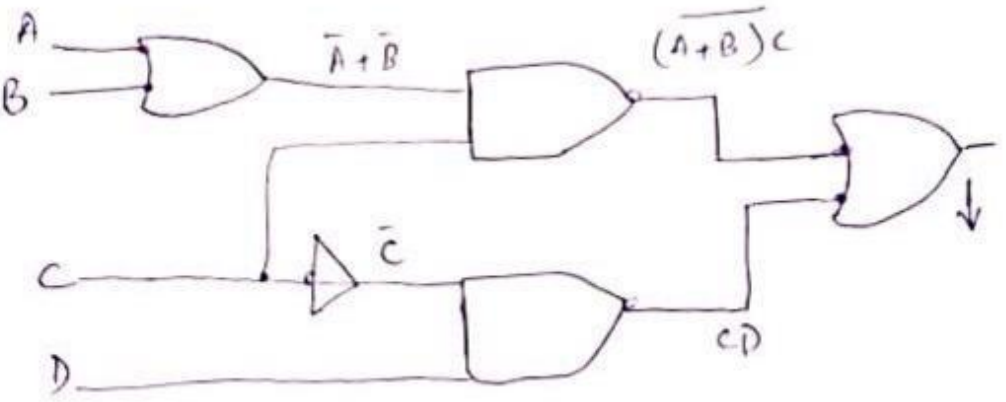
Q1 Diagram



$$X = (\overline{A+B})C + C\bar{D} = (\bar{A}+\bar{B})C + C\bar{D} + A\bar{C} + \bar{B}C + \bar{C}D$$

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Q9. For the 4 input multiplexer, data inputs are given as.

$D_0 = 0, D_1 = 1, D_2 = 0, D_3 = 1$

Find the output Y if the select inputs are given as

(a) $S_0 = 1, S_1 = 0$

(b) $S_0 = 0, S_1 = 1$

(c) $S_0 = 1, S_1 = 1$

(d) $S_0 = 0, S_1 = 0$

(a) $S_0 = 1, S_1 = 0$

In case of 4x1 multiplexer when $S_0 = 0$ and $S_1 = 0$ then the output is D_0

S_0	S_1	Output
0	0	D_0

So output is 0.

(b) $S_0 = 0, S_1 = 1$

S_0	S_1	output
0	1	D_1

So output is 1 as $D_1 = 1$

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(c) $S_0 = 1, \quad S_1 = 1$

S_0	S_1	output
1	1	D_3

So the output is $D_3 = 0$

(d) $S_0 = 0, \quad S_1 = 0$

S_0	S_1	output
1	0	D_2

So the output is $D_2 = 1$

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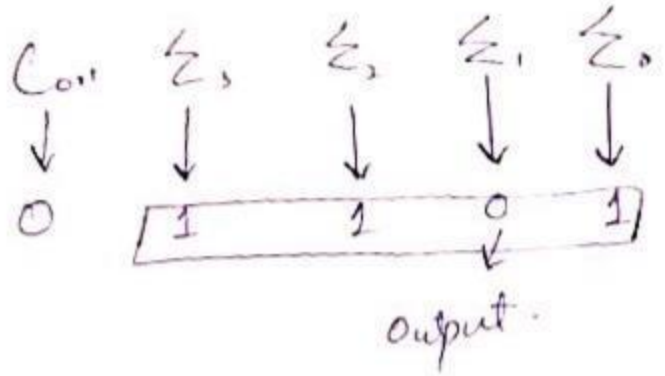
Q3: For the circuit in figure 03, assume the 03 inputs are Add/Subt = 1, A = 1010, and B = 1101. what is the output?

Ans The output of the circuit is:



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Q4: Determine the A-B, A>B, and A<B outputs for the inputs numbers shown on the comparator. (8)

Ans: Solution:

The number on the A inputs is 0110 and the number on the B inputs is 0011. The A>B output is HIGH and the other outputs are Low.

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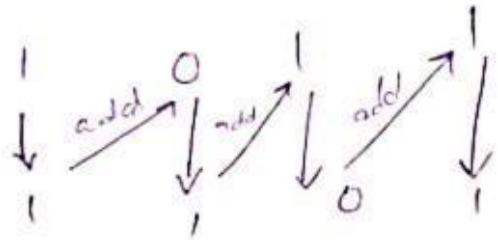
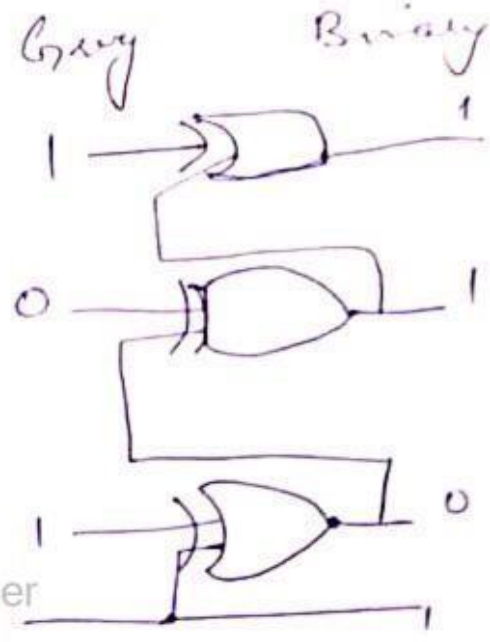
Q5 Show the logic required to convert a 4-bit gray code to binary and use that logic to convert the following gray code words to binary 1011.

Ans: The logic to convert gray to binary is shown below.

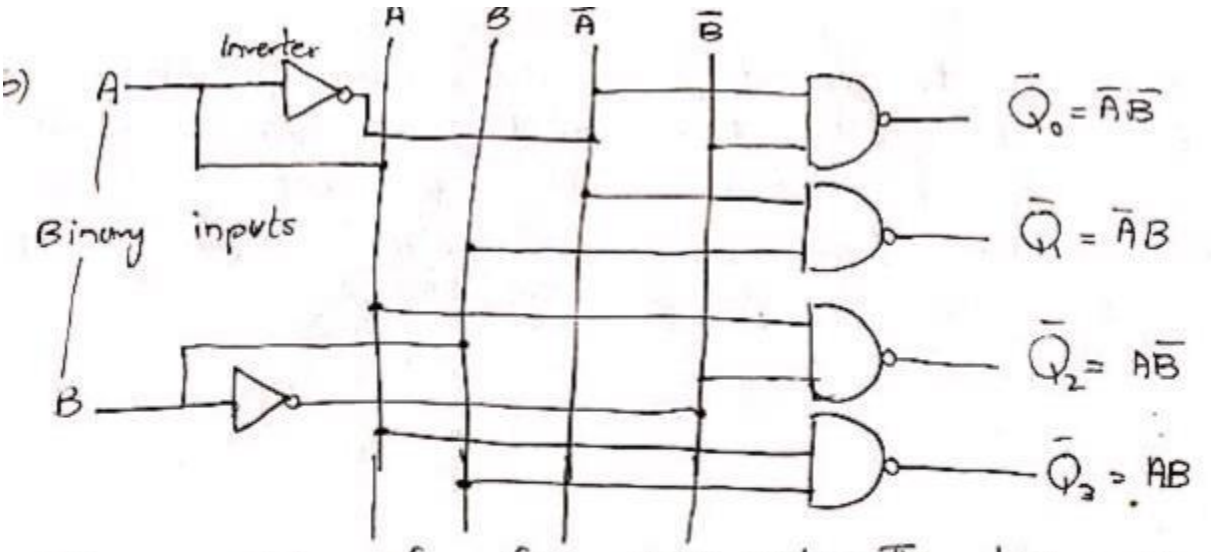
1011 → gray code.



Binary = 1101



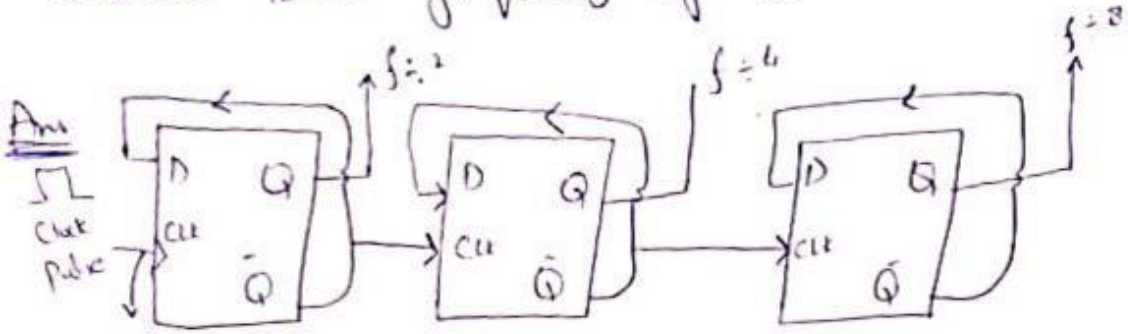
Question No 6



This consists of four AND gates. The binary 2 inputs A & B are decoded into one of 4 outputs, hence description of 2- to 4- binary decorder.

Q7 Draw and explain the logic diagram for frequency divider (use 3 J-K flip-flop) assume 16 kHz frequency of the initial wave form. (5)

Ans



initial waveform. (frequency output) f_0.

We used three frequencies divider (3 Toggle JK flip flops circuit). Initial waveform is of 16 KHz and output from first toggle flip flop (frequency divider) is 8 kHz and so on. At the last frequency is 2 kHz.

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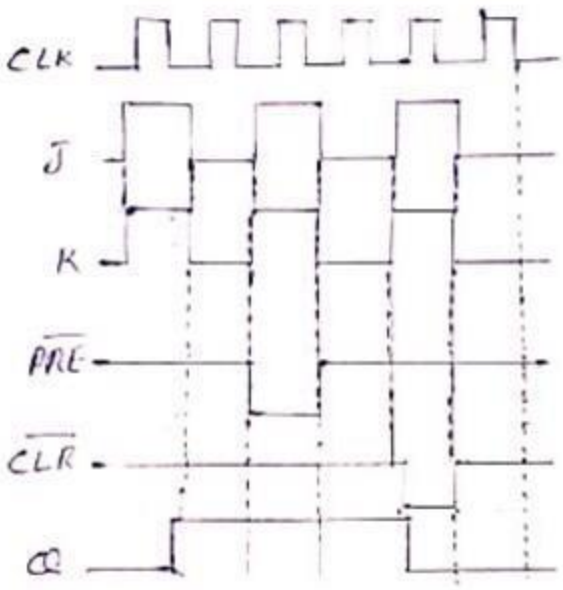
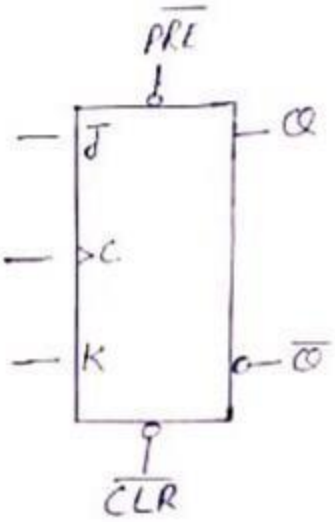
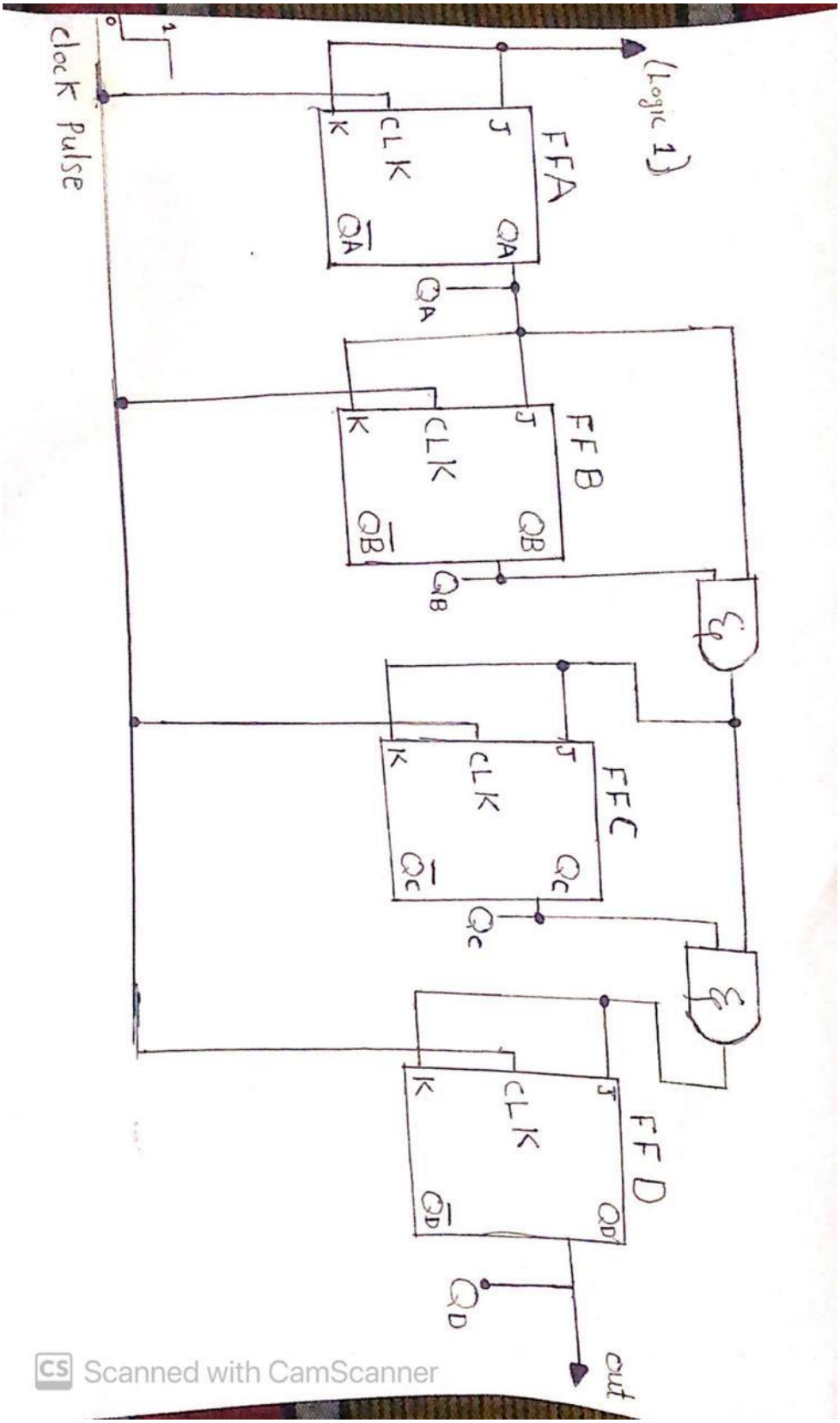
Q8:- Determine the Q waveform relative to the clock if the signals shown in Figure 04 are applied to the Inputs of the J-K flip-flop. Assume that Q is Initially Low.

Ans:-





Question No 9



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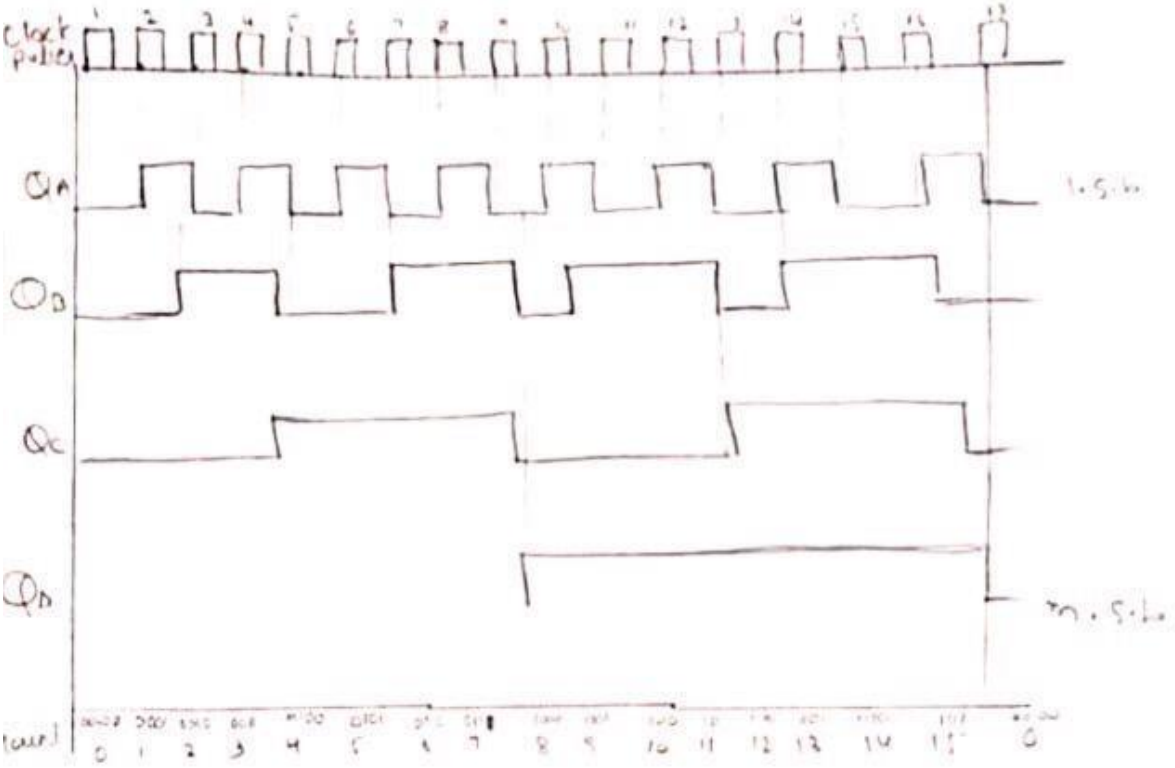
4-bit Synchronous Counter Waveform



Because This 4-bit synchronous counter counts sequentially on every clock pulse the resulting output count upwards from 0 (0000) to 15 (1111). Therefore, This type of counter is also known as 4-bit synchronous up counter

However, we can easily construct a bit 4-bit synchronous Down counter by connecting