NAME :- MUHAMMAD FAIZAN

ID NO :- 13205

SUBJECT :- ELECTRONIC DEVICE AND CIRCUIT

DEPARTMENT :- ELECTRICAL ENGINEERING

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SUBMITTED TO :- Dr. Shehyar Shafiq

Muhammad Faizan
ID No# 13205

Question # 1

Solution:
The 1N4747 zener diode used the regulation circuit in figure is 20V.

$V_Z = 20V$ $I_Z = 12.5mA$
$I_{ZK} = 0.25mA$ $Z_Z = 22\Omega$

Part
(a) For I_{ZK}

$$V_{out} = V_Z - \Delta I_Z - I_Z$$
$$= 20V - (I_Z - I_{ZK}) Z_Z$$
$$= 20V - (12.5mA - 0.25mA) 22\Omega$$
$$= 20V - (12.25mA) 22\Omega$$
$$= 20V - 0.267V$$

$$V_{out} = 1973V$$

Calculate the zener diode maximum current the power dissipation is 1w

$$I_{ZM} = P_{D(Max)} / V_Z = 1w / 20V = 50mA$$

For I_{ZM}

$$V_{out} = V_Z + \Delta I_Z Z_Z$$
$$= 20V + (I_{ZM} - I_Z) Z_Z$$
$$= 20V + (50mA - 12.5mA) 22\Omega$$
$$= 20V + (37.5mA) 22$$
$$= 20V + 0.825$$
$$V_{out} = 20.825V$$

Part

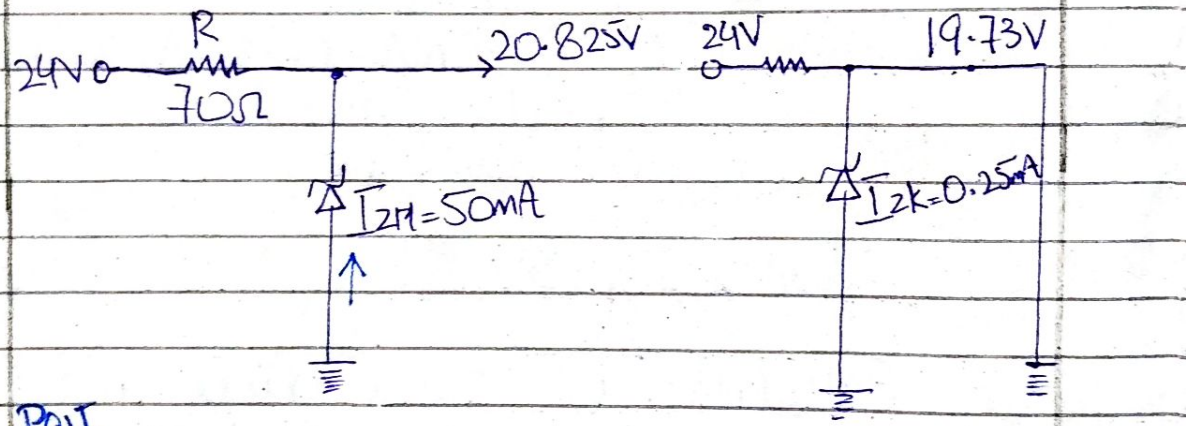
(b) Calculate the value of R for maximum zener current when there is no load as shown in figure,

$$R = \frac{V_{IN} - V_{out}}{I_{zm}}$$

$$= \frac{24V - 20.825V}{50mA}$$

$$R = 63.5\Omega$$

$R = 70\Omega$ (Nearest largest standard)



Part

(c) For maximum load resistance (maximum current). The zener diode current minimum ($I_{zk} = 0.25$)

$$I_T = V_{IN} - V_{out}/R$$

$$= \frac{24V - 19.73V}{70\Omega}$$

$$= 0.061A$$

Question # 2

(2) Determine I_B, I_C, I_E, V_{BE}, V_{CE}, V_{CB} in the circuit shown in Fig: 2.

⇒ Solution:

$$V_{BE} = 0.7V$$

$$\Rightarrow I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5V - 0.7V}{3.9k\Omega} = \boxed{1102\mu A}$$

$$\Rightarrow I_C = \beta_{DC} I_B = (150)(1102\mu A) = \boxed{165.3mA}$$

$$\Rightarrow I_E = I_C + I_B = 165.3mA + 1102\mu A = \boxed{166.4mA}$$

Solve for V_{CE} & V_{CB}

$$V_{CE} = V_{cc} - I_C R_C = 15V - (165.3mA)(180\Omega)$$
$$= 15V - 29.7V = \boxed{-14.7V}$$

$$V_{CB} = V_{CE} - V_{BE} \Rightarrow -14.7V - 0.7V$$
$$\boxed{= -15.4V}$$

Since the collector is at a lower voltage than the base, the collector-base junction is forward biased.

Question # 3

Answer :

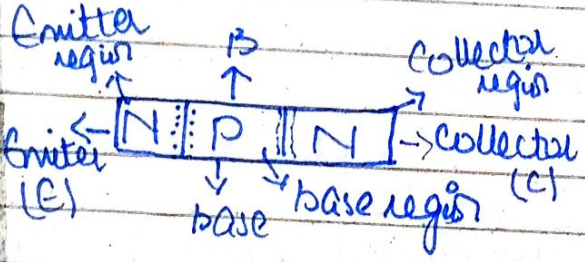
Bipolar Junction Transistor :

⇒ BJT :

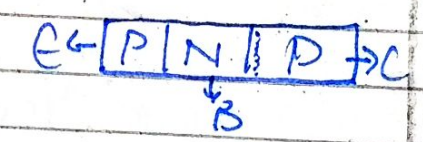
- It is invented in Dec 1947 at bell labs at USA.
- BJT is a three terminal device and it is used in amplification of weak signals and for switching purpas.

⇒ Physical structure :-

NPN

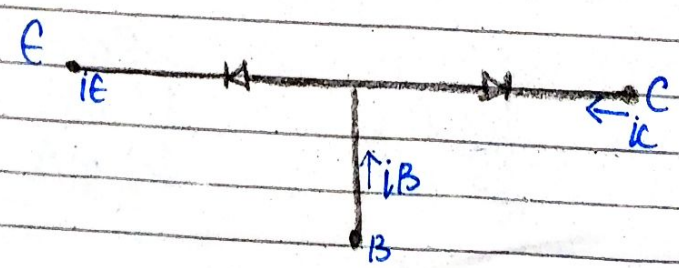


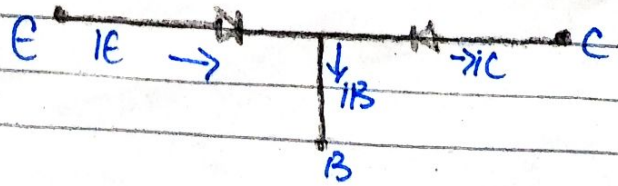
PNP



→ 2 Junction N
→ 1 Junction P
→ J_1 → emitter base
→ J_2 → Collector base
→ There is a depletion region at J_1
→ There is a depletion region at J_2

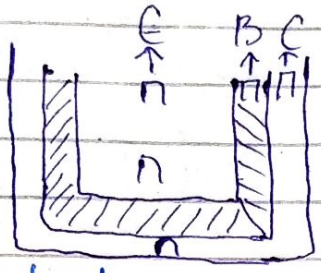
width C > E > B
doping E > C > B

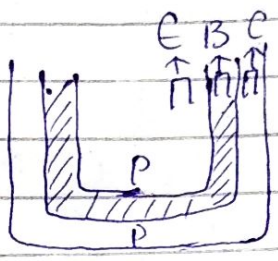




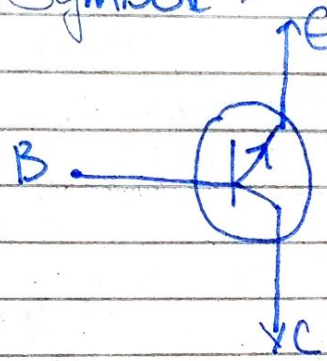
Cross section view :-

NPN

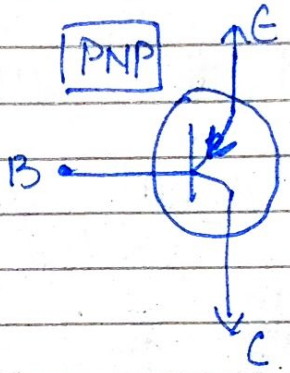




Symbol :-



PNP



• Increase of NPN there will be more from B → E.

⇒ Now using the relationship $I_C = \beta_{DC} I_B$ value of I_C are calculated and tabulated in below table.

⇒ The resulting curves are :-

Table :-

I_B	I_C
5 μA	0.5 mA
10 μA	1.0 mA
15 μA	1.5 mA

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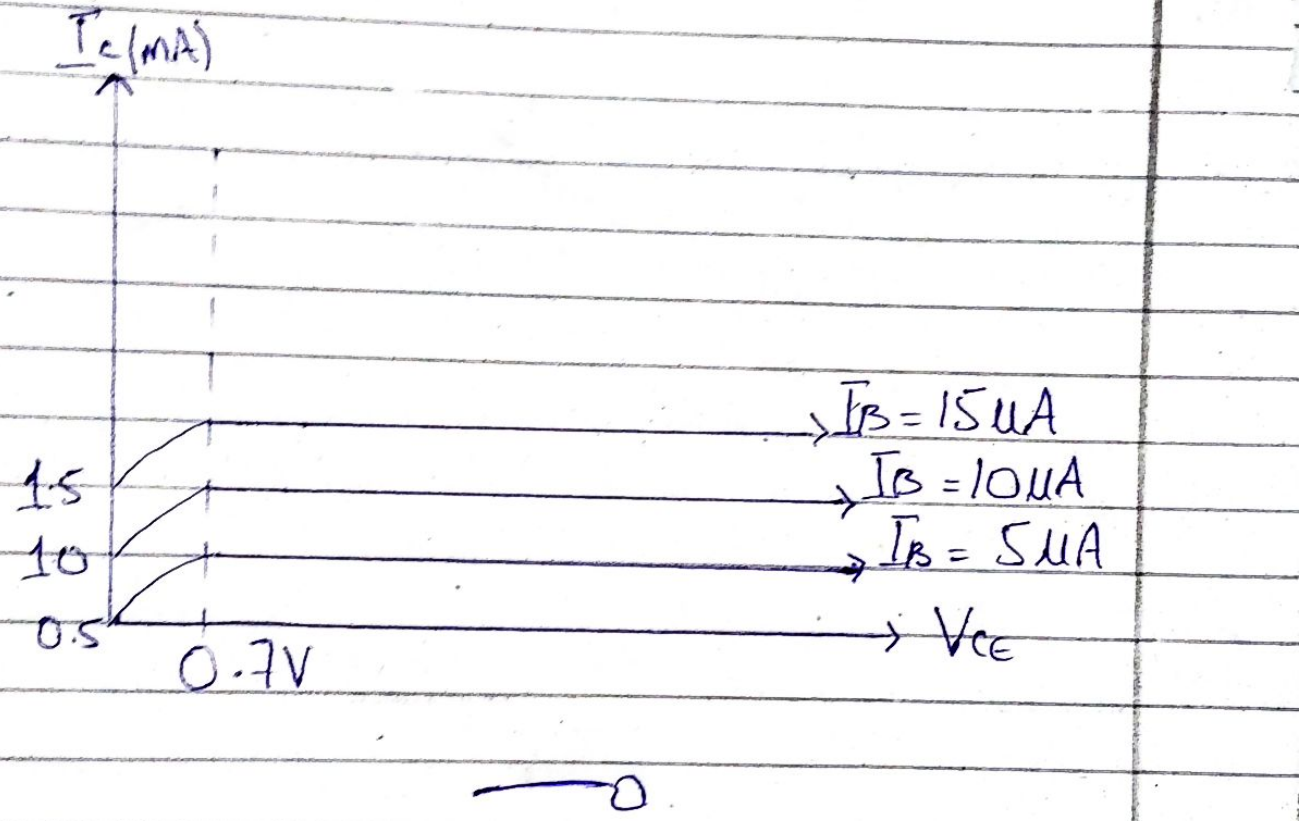


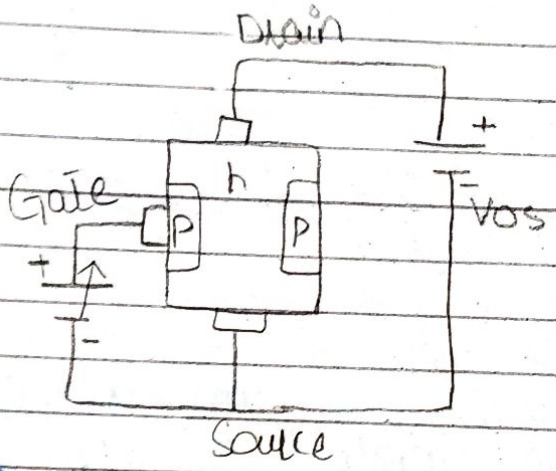
Question #4

Q4: For a transistor to act as a switch, you need to join each of the following conditions on left to ON or OFF state.

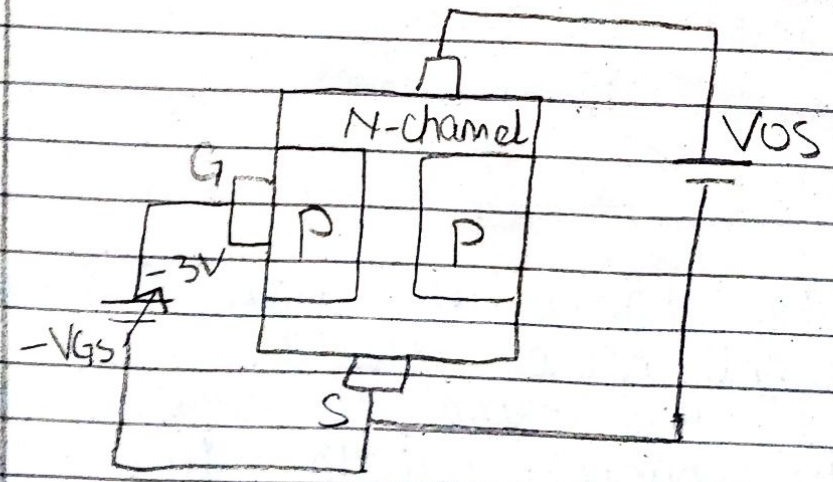
Transistor Fully ON (ON)
Transistor Fully OFF (OFF)
Input and base are at 0V (OFF)
Collector current $I_C = 0$ (OFF)
$V_{CE} = V_{cc}$ (OFF)
BE junction is reverse bias (OFF)
BC junction is forward bias (OFF)
Maximum or saturation current I_C flows (ON)
BE junction is ~~formed~~ forward bias (ON)
BC junction is forward bias (ON)
$V_{CE} = 0V$ (ON)
BE junction is less than 0.7V (OFF).

Question # 5

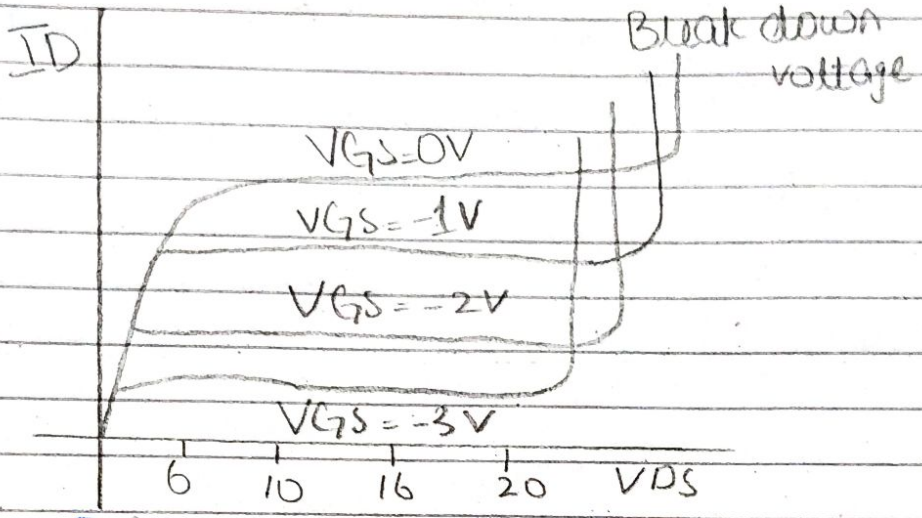
Ans :- JFET is a type of junction field effect transistor which is voltage controlled device as differ from BJT which is current controlled.



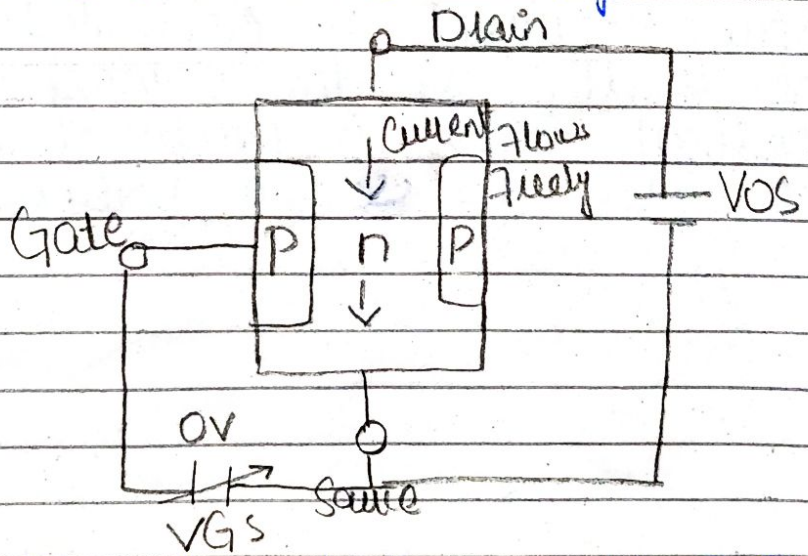
Actually in FET the drain to source current is controlled by the width of the channel the electrical field is produced by the gate to source voltage.



So, V_{GS} is more negative so no current flows and this effect is called Pinch off region no current or less current flows.



So, if we see the graph with no voltage applied to the gate, the current flows freely.



⇒ The channel are wider & Drain current moves freely.

⇒ If we move to negative value the channel width starts to decrease and current cannot moves.

Question #6

Given data :-

$B_{DC} = 125$ $\quad V_{CE(sat)} = 0.4V$

$V_{CC} = 10V$ $\quad R_C = 1k\Omega$

* Required :-

$V_{CE} = ?$

Solution :-

Part (a) :-

When $V_{IN} = ON$ so transistor is in cutoff mode and

$V_{CE} = V_{CC} = 10V$

Part (b) :-

min $I_B = ?$, $B_{DC} = 125$, $V_{CE} = 0.4$

$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{10V}{1k\Omega} = 10mA$$

$$I_{B(min)} = \frac{I_{C(sat)}}{B_{DC}} = \frac{10mA}{125} \Rightarrow 80\mu A.$$

Question # 7

Q(7) Determine ripple factor for the filtered bridge rectifier with a load as indicated in Figure 4.

⇒ Solution:-

Turn ratio = 0.1

Peak Primary voltage is = $V_{p(pri)} = 1.414 V_{rms}$

$= 1.414(120) = 170V$

Peak secondary voltage is = $V_{p(sec)} = n V_{p(pri)} = 0.1(170)V = 17V$

Unfiltered peak full wave rectified voltage =

$V_{p(rec)} = V_{p(sec)} - 1.4V = 17V - 1.4V = 15.6$

Frequency of full wave rectified voltage = 120Hz

Peak to Peak ripple voltage at output

$= V_{r(pp)} = \left(\frac{1}{fR_L}\right) V_{p(rect)}$

$= \left(\frac{1}{(120Hz)(3300\Omega)(100uf)}\right) 15.6 = 0.393V$

DC value of output voltage =

$V_{DC} = \left(1 - \frac{1}{2fR_LC}\right) V_{p(rect)}$

$= \left(1 - \frac{1}{(240Hz)(3300\Omega)(100uf)}\right) 15.6 = 15.4V$

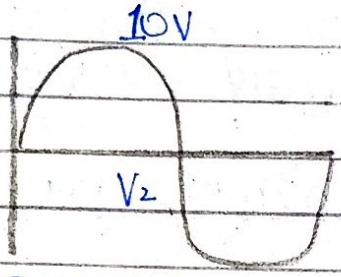
Ripple factor result = $r = \frac{V_{r(pp)}}{V_{RC}} = \frac{0.393V}{15.4V} = 0.025$

Ripple factor = **2.5%**

Question # 8

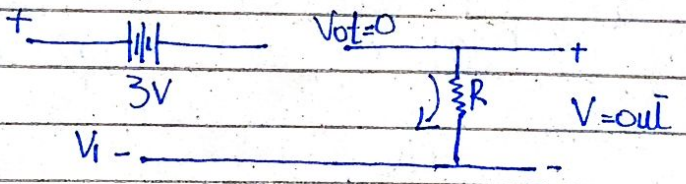
Q8 :- Determine the output voltage waveform for the circuit given in figure 5.

⇒ Solution :-



$V_i + 3V = 0V$

$V_i = -3V$



$V_O = V_R = I_R(R) = 0(R) = 0$

$V_O = V_i + 3V$

Transition voltage

$V_i + 3V = 10V + 3V = 13V$

$V_O = 0V + 3V = 3V$

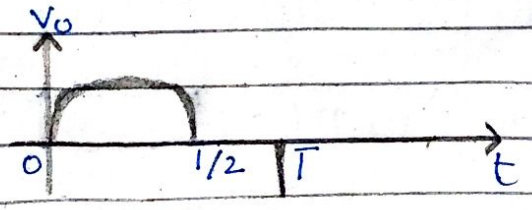
$V_O = -3V + 3V = 0$

Output :-

$V_i + 3V = 10 + 3V = 13$

$V_i = 0V + 3V = 3V$

$V_O = -3V + 3V = 0V$



Question # 9

Q9:- Determine the output voltage waveform for the circuit given in Fig:6. Assume RC time constant is much greater than the period of the input.

⇒ Solution :-

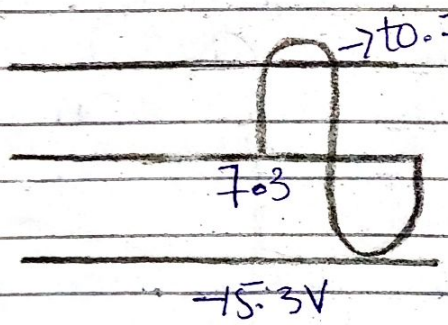
As we know

⇒ $V_{DC} \cong -(V_{p(in)} - 0.7V) = -(8V - 0.7V) = -7.3V$

⇒ The output wave form goes upto +0.7V approximately

⇒ The output voltage will have an average value of slightly less than calculated

So, the wave form will be



Output voltage waveform

① 10 :-

(10) Answer the following questions:-

(a) Power supply filters (capacitors) are used to smooth the pulsating DC output after rectification so that a nearly constant DC voltage is supplied to the load. It reduces the amount of ripple voltage to a level that is acceptable.

Operation :-

⇒ In a filter circuit the capacitor is charged to the peak of the rectified input voltage during the positive portion of the input. When the input goes negative, the capacitor begins to discharge into the load. The rate of discharge is determined by the RC time constant formed by the capacitor and the load resistance.

⇒ The capacitance needed to supply the power supplies output current with specified amount of ripple current (Vrms) with full wave rectification is :-

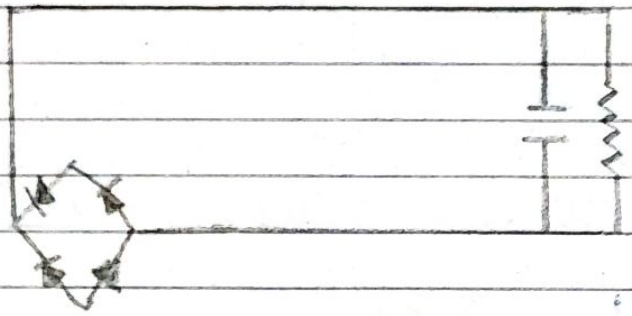
$$C = \frac{1}{V_{rms} \times A} \quad \text{where } V_{rms} = \frac{V_{(p-p)}}{2} \text{ for } f = 60Hz$$

$C = \frac{2.4 I}{V_{rms}}$ I = DC load current of power supply

A more general formula :-

$C \sim \frac{I \times V_{ac}}{V_{rms} V_m}$ where $V_{ac} = \frac{V_m - V_{p-p}}{2}$

V_m = max voltage of input wave form
V_{p-p} = peak to peak ripple voltage



Part

(b) There are two types of semi-conductor.

* Intrinsic
* Extrinsic

⇒ There are further two types based upon the type of impurity added

1) N - Type
2) P - Type

* Formation of N-type semi-conductor:

⇒ N-type semi conductor is doped with the pentavalent impurity like phosphorus antomny and arsenic. The impurity is added in very minute amount. The pentavalue impurity makes

covalent bond with silicon atoms and electron isn't bonded with any Si atoms each penta valent elements impurity donates one e⁻ to the N-type semi conductor and is called donar impurity & in this type electrons are main conductor of current.

⇒ Formation of P-type semi conductor:-

⇒ The P-type is formed when a tri-valent impurity is added to a pure semi-conductor. In result large number of holes created acts as carrier. These impurities are called accepter impurities such as galium and indium.

—o

Part

(c) Diode limiters

It is a circuit in which it takes an input wave form and cuts off its top-half, bottom half or both together & produces wave forms that ~~reduces~~ resembles flattened version of the input.

⇒ Positive diode limiter:-

In the diode limiting circuit the diode is forward biased. For the diode to become forward biased it must have the input voltage magnitude greater than +0.7 volts. A voltage bias is added in series with the diode.

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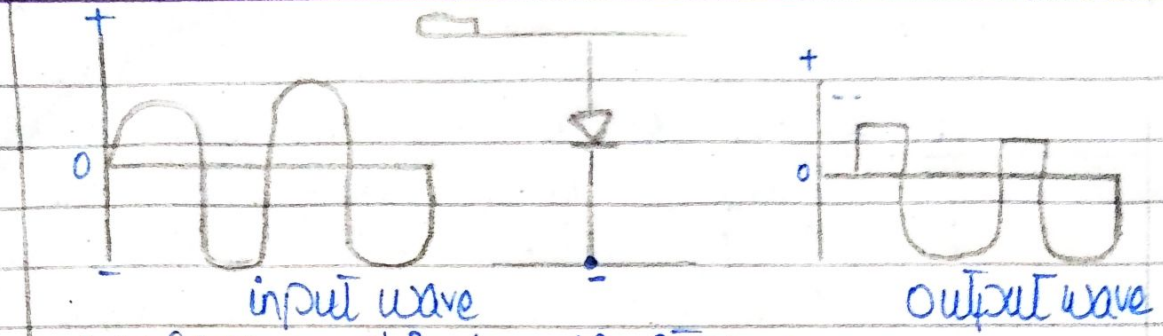
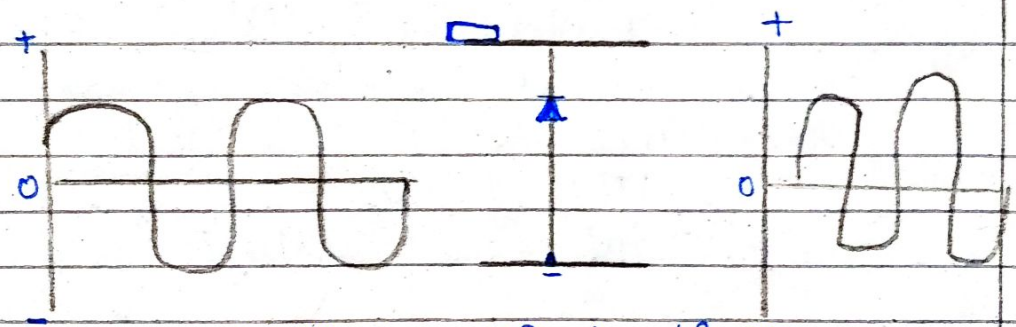
(positive diode limiter) (17)



input wave output wave

x Negative diode limiter :-
when the diode is ~~turned~~ forward biased during a negative half of the cycle and limits it 0.7 V while allowing the positive half of the cycle is called negative limitors of the circuit.
⇒ the output wave form is held to a level-bias of.



Negative diode limiter

Part (D) Capacitor effectively act as a battery in clamping circuit.

Part (E) The input frequency of half wave rectifier is same to input frequency so if 60Hz sinosidal voltage is applied than the output also 60Hz.

Part

(f) Zener diode is a PN Junction diode specially manufactured to have some desired operation when reverse biased.
⇒ In forward bias Zener diode behaves as a Normal PN Junction diode and drops 0.3 volt for Germanium based & 0.7 volt for Silicon based Zener diode.

Part

(g) The magnitude of the current flowing through the channel between the Drain and the source terminals is controlled by a voltage applied to the Gate terminal which is a reverse biased. In an N-channel JFET this Gate voltage is negative while for a P-channel JFET the Gate voltage is positive.