Student Details

Name: khalid khan **Student ID:** 13880

Q 1.		Design an area efficient layout diagram for the CMOS logic shown below F= AB+(CD)E
Q 2.		Give the subsystem design considerations of a four-bit adder.
Q 3.		Discuss the VLSI design issues and design trends. Explain with neat diagram, simple parity check code.
Q 4		Does the inverter with a lower VOL always have the shorter high-to-low switching time? Justify your answer.
Q 5.		Design 8×1 MUX using two 4:1 MUX and one 2:1 MUX along with its diagram. Implement 8×1 multiplexer in VHDL using structural modelling style. **GOOD LUCK**

Name = Khalid Khan Page = 1 13880

Q No-1

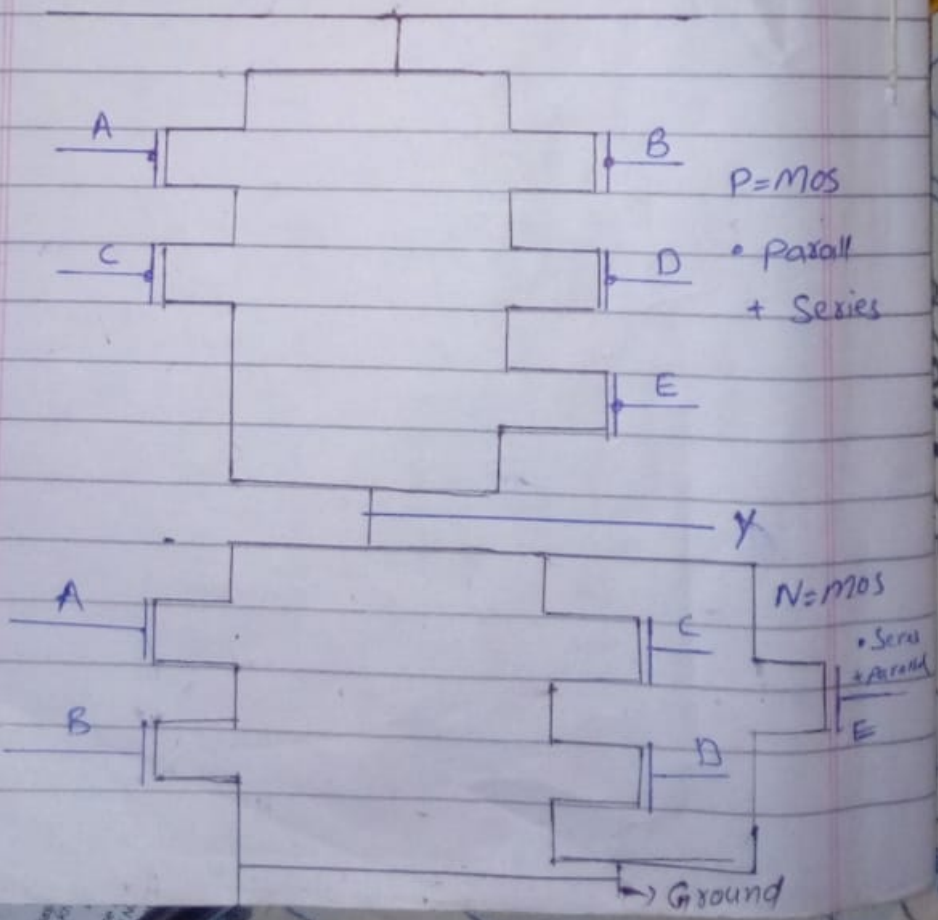
Design an area efficent layout for the CMOS shown below

$F = AB + C(D)E$

N = • Series
+ Parallel

P = • Parallel
+ Series

$F = A \cdot B + C(C \cdot D)E$

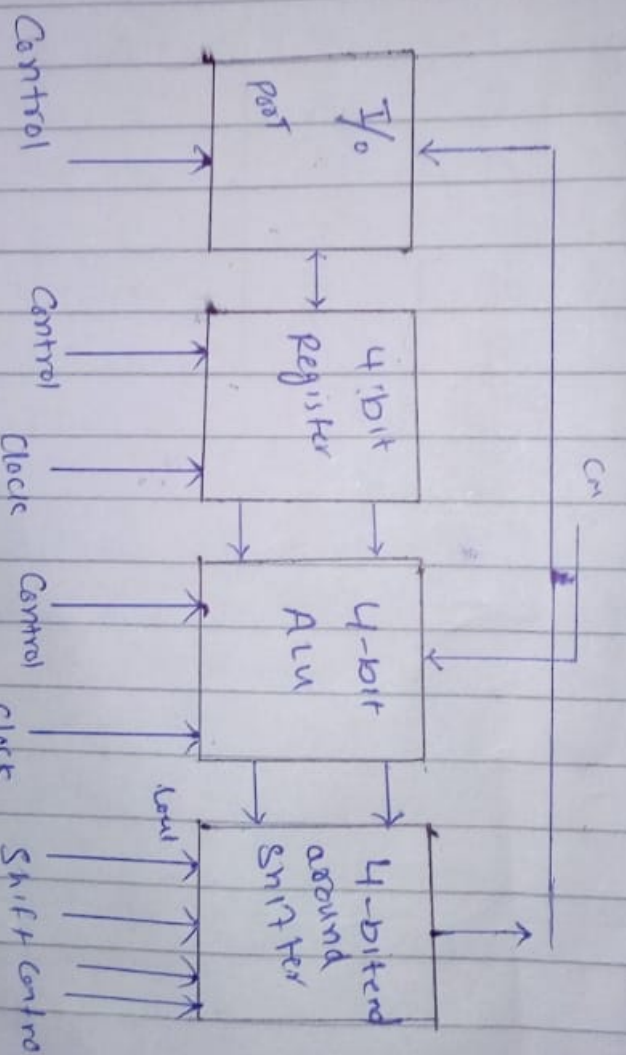


Name = Khalid khan Page = 2 13880

Q(a) Give the subsystem design Consideration of a four-bit adder

Ans:→

design Subsystem design Consideration



Name = Khalid Khan Page = 3 13880

=> Design 4-bit adder

INPUTS			OUTPUTS	
AK	BK	CK-1	SK	CK
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

Subsystem design Considerations of a four bit adder

we are explain by Throuth table

Q3 Discuss the VLSI design issues and design trends

Ans ⇒

VLSI design issues

=> Realize a given Specification on silicon optimizing the following features

(1) Speed
(2) Testabality
(3) design time
(4) Power dissipation
(5) Area

These five issues g discuss in VLSI design

=> VLSI design trends

P.T.O →

VLSI design trends

There are many trands in VLSI design

=> processor,
=> memory
=> Iso devices
=> computer hardware
=> Computer Software
=> Telecommunications
=> Data bases
=> ware houses etc.

Q (3) (B)

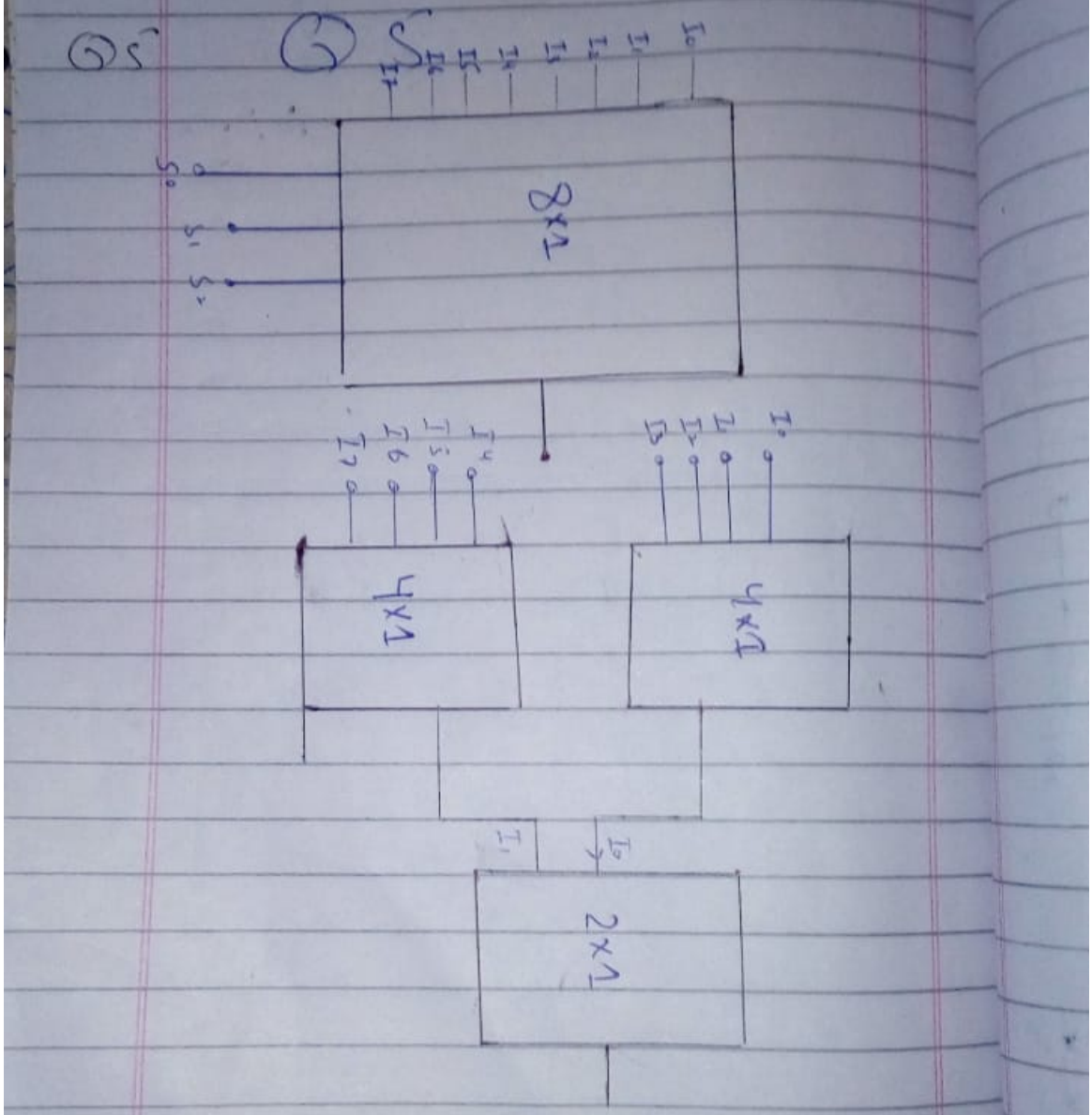
Explain with neat diagram, Simple Parity code.

Q 4

Ans⇒

The inverter have always Lower limit of power depends on the sum of the Threshold voltage of the NMOS and Vdd

* Logic Function is implemented by pull-down network only
* full Swing out put Cvoltage and Vot = VDD
* Non - ratioed
* Faster swteching speeds.


8x1
4x1
4x1
2x1
S0
S1
S2

Khalid Khan Page 9 13880

8×1

Truth table

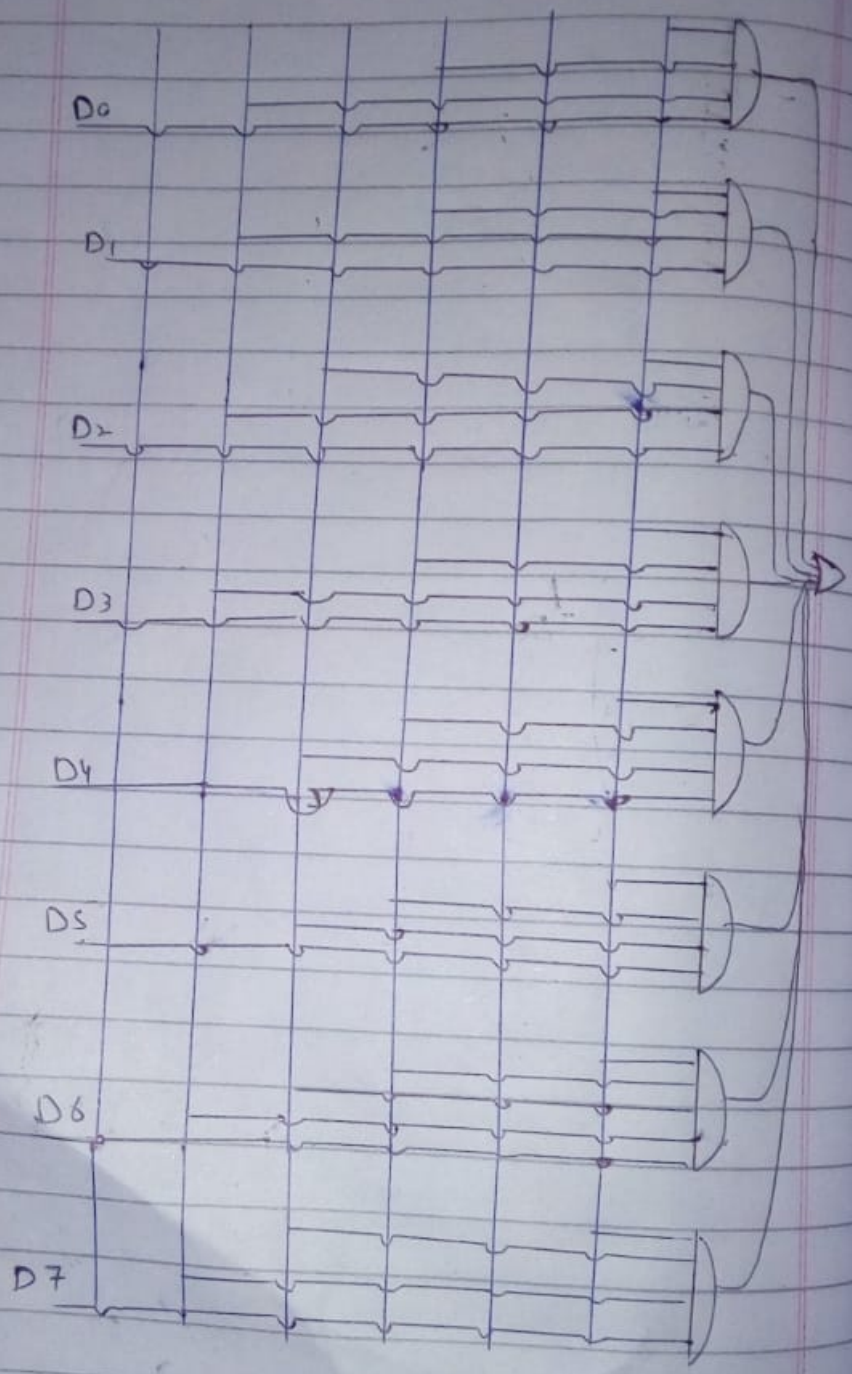
S_2	S_1	S_0	Output
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

4×1

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

2×1

S_1	S_0	Y
0	0	I_0
0	1	I_1


D0
D1
D2
D3
D4
D5
D6
D7

Khalid Page 11 13880

8x1 MUX By VDHL Method

$I_0 = S_2 \; S_1 \; S_0$

$I_1 = S_2 \; S_1 \; S_0$

$I_2 = S_2 \; S_1 \; S_0$

$I_3 = S_2 \; S_1 \; S_0$

$I_4 = S_2 \; S_1 \; S_0$

$I_5 = S_2 \; S_1 \; S_0$

$I_6 = S_2 \; S_1 \; S_0$

$I_7 = S_2 \; S_1 \; S_0$