M- Amin Sir,

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Sub # Computer architecture

Dept # BS(CS)

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Q (1)

Ans (a) Word:

The natural unit of organization of memory. The size of word is typically equal to the number of bit used to represent an integer and to the instruction length. Unfortunately there are many exceptions. For example CRAY (90 has a 64-bit word length but uses a 46 bit integer representation. The intel x86

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architecture has a wide variety of instruction lengths expressed as multiple of bytes and a word size of 32 bits.

Addressable Unit :-

In some systems, the addressable unit is the word. However, many systems allow addressing at the byte level. In any case the relationship between the length in bit A of an address and the number N of addressable unit is $2^A = N$.

Unit of transfer :-

For main memory this is the number of bits read out of or written into memory at a time the unit of transfer need not equal a word an addressable unit. For external memory data are often

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transfered in much larger units than a word, and these are refered to as blocks.

(b)

Ans: Least Recently used (LRU) :-

Least Recently used (LRU) in easily implemented by two way set association mapping Each line include a use bit. When a line is refrenced, its use bit is set to 1 and use bit of the other line is that set is set to 0. When a block is to be read into the set the line whose use bit is 0 is used. Because we are assuming that more recently used memory locations are more likely to be refrenced. LRU should give the best hit ratio.

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Least Frequently Used (LFU):-

FLU

Could be implemented by associating a counter with each line.
A technique not based on usage (i-e not LRU, LFU, FIFO & Sense variation) is to pick a line at random from among the candiate lines. Simulation Studies have shown that random replacement provides only slightly inferior Performance to an algorithm based on usage.

C

Ans. Read operation:-

In SRAM for any operation to be Performed the word line should be high To Perform read operation initially

Write operation:-

Consider the memory bit consists of Q = 0 and Q' = 1

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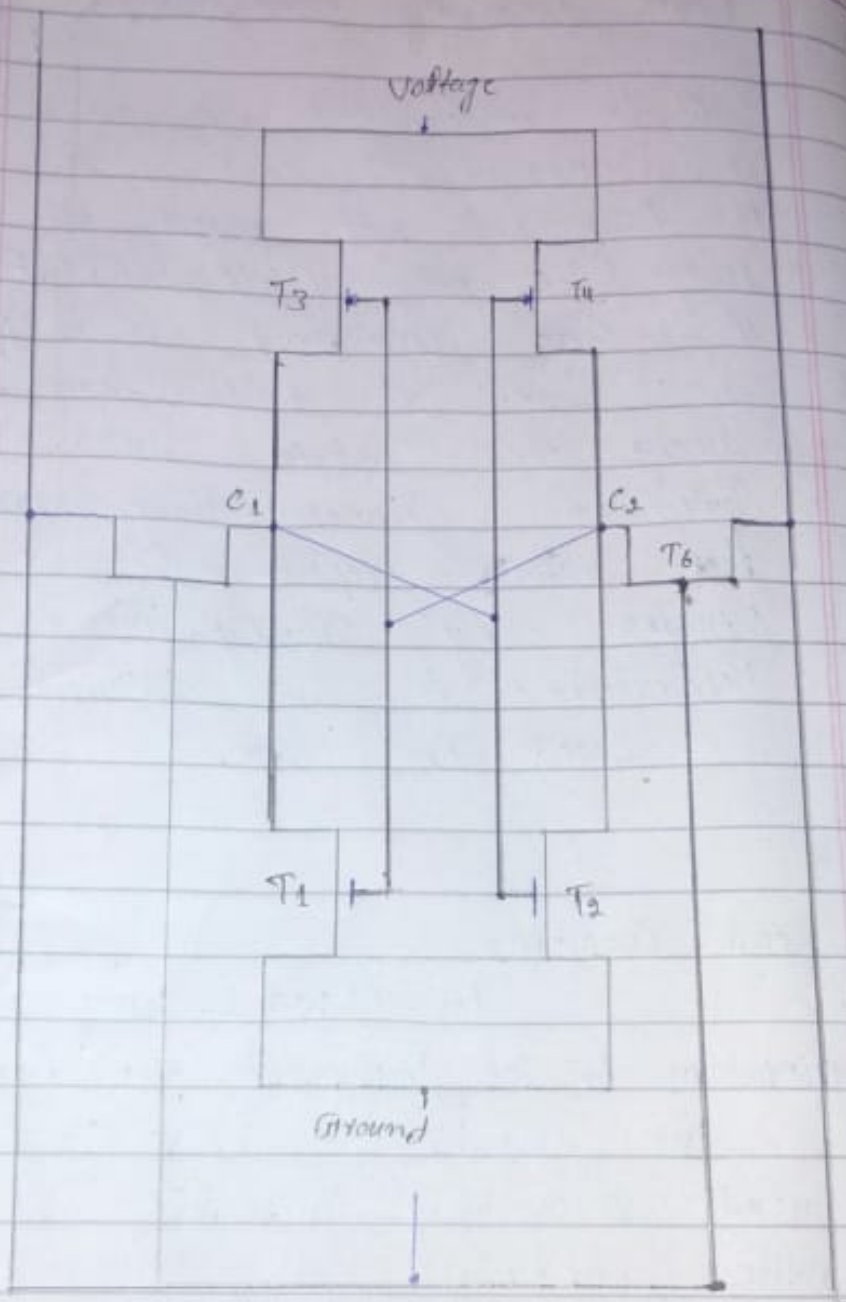

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16 M bit DRAM:-

In this Case 4bits are reads or written at a time. Logically the memory array is organized as four Square arrays of 2048 by 2048 elements. Various physical arrangement are possible. In any Case, the element of the array are Connected by both horizontal line Connected to the ~~b~~ Select terminal of each cell in its row, each vertical lines Connects to the Data - In/Sense terminal of each cells in its Column.

~~Beause~~ Because only 4 bits are read - written to this DRAM. there must be multiple DRAMs Connect to the memory Controller to read/ write a word of data to the bus

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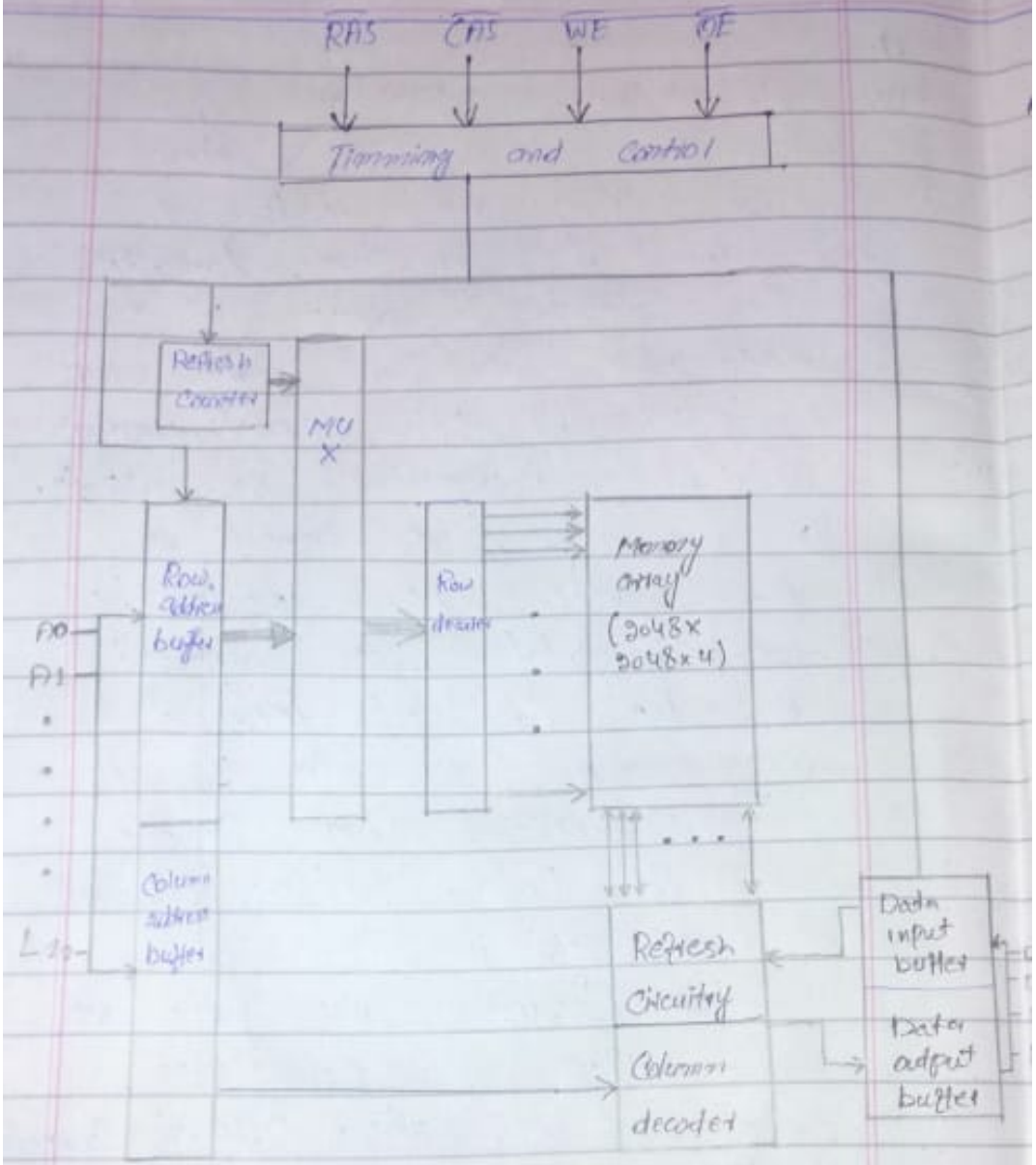

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(c)

Ans: The DVD's greather capacity is due to three differences from CDs.

(1) Bits are packed more closely on a DVD. The spacing between loops of a spiral on a CD is 1.6 μm and the minimum distance between pits along the spiral is 0.834 μm.

(2) The DVD employs a second layer of pits and lands on top of a first layer. A dual layer DVD has a semireflective layer on top of the reflective layer by adjusting focus, the laser and DVD drives can read each layer separately.

(3) The DVD-ROM can be two sided, where as data is recorded on only one side of CD. This brings total capacity upto 17 GB.

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2 (a)

3 (a) EEPROM :-

Electrically erasable programmable read - only memory (EEPROM) is a read - mostly memory that can be written into at any time without erasing prior contents only the byte or bytes addressed are updated, The write operation takes considerably longer than the read operation, on the order of several hundred micro second per byte. EEPROM is more expensive than EPROM and also is less dense supporting fewer bits per chips

Flash memory :

Flash memory is intermediate between EPROM and EEPROM in both cost and functionality. Like EEPROM, flash memory uses and electrical erasing technology. An entire flash memory can be erased in one or

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a few seconds, which is much faster than EPROM. Flash memory does not provide byte-level erase.

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b)

(b) Hard failure:-

A hard failure is a permanent physical defect so that the memory cells are cells affected cannot reliably store data but become stuck at 0 or 1 or switch erratically between 0 and 1. Hard errors can be caused by harsh environment abuse manufacturing defects and wear.

Soft error:

A soft error is random nondestructive events that alters the contents of one or more memory cells without damaging the memory. Soft errors are caused by

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Power Supply Problems of alpha Particles. These particles result from radioactive decay and are distressingly Common because radioactive nuclei are found in small quantities in nearly all materials.

(c) Magnetic Disk

Read Mechanism:-

The traditional read mechanism exploits the fact that a magnetic field moving relative to a coil produces an electrical current in the coil. When the surface of the disk rotates under the head it generates a current of the same polarity as the one already recorded.

Write Mechanism:-

The write mechanism exploits the fact that electricity flowing through

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a coil produces a magnetic field. Electric pulses are sent to the write head, and the resulting magnetic patterns are recorded on the surface below with different patterns for positive and negative currents.

d)

(J) Parallel Access:-

All number disks are participate in the execution of every I/O request. Typically, the spindles of individual drives are synchronized so that each disk head in the same position on each disk at any given time.

Independent Access:-

Each number disk operates independantly. So that separates I/o request can be satisfied in parallel.

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(e)

(e) HD DVD:-

- The HD DVD scheme can store 15 GB on a single layer on a single side.
- HD DVD players have been much cheaper than Blu-ray machines.
- It delivers sharp resolution.
- It is cheaper than Blu-ray.

BLU-ray DVD:-

- Blu-ray discs have more storage space and more advanced protections against piracy
- It also deliver sharp resolution.
- Blu-ray has 25 GB capacity and is more expensive than HD DVD.

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Q 3 (a)

Ans (a) Memory ~~Acc~~ access Methods:-

(*) Sequential Access:-

Memory organized into units of data called records. Access must be made in a specific linear sequence. Stored addressing information is used to separate records and assist in the retrival process. A shared read-write mechanism is used, and this must be moved from its current location to the desired location, passing and rejecting each intermediate record Tape visit are Sequential access

* Direct Access:-

As with Sequential access direct access involves Shared read write mech mechanism. However, individual blocks or record have a unique address based on physical location access

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time is variable Disk units are direct access.

* Random Access: The time to Access a given location is independent of the sequence of prior accesses and is constant Thus any location can be selected at random and directly addressed and accessed. Main memory and some cache system are random access.

2-(b) Principal of Locality:

The Principal of locality also known as locality of reference, is the tendancy of a processor to access the some set of memory location repetitively over a short period of time There are two basic type of Principal of locality.

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(a) Temporal Locality:-

It refers to the re-use of specific data and/or resources, within a relatively small time duration.

(b) Spatial Locality:-

It is also known as data locality. It refers to the use of data elements within relatively close storage location.

(C)

(C) Possible approaches to cache coherency:-

Possible 4 approaches to cache coherency include the following.

Bus watching with write through:-

Each cache controller monitors the address lines to detect write operation to memory by other bus masters. If another master writes to a location in shared

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that also reside in the Cache memory, the Cache Controller invalidates that Cache entry.

- Hardware Transparency:-

Additional hart-ware is used to ensure that all updated to main memory via Cache are reflected in all Cache.

- Noncacheable Memory:-

only a portion of main memory is shared by more than one processor, and this is designated as non-Cacheable The noncacheable memory can be identified using chip-Select logic or high-address bits.

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(d)

Ans:(d) Practical issues peculliar to SSDs:-

There are two practical issues peculliar to SSDs that are not faced by HDDs.

(1) First SSD performance has a tendancy to slow down is the device is used. To understand the reason for this, you need to know that files are stores on disk is a set of pages, typically 4KB in length. These page are not necessarily, and indeed not typically stored as a ~~Configuous~~ Configuous set of pages on the disk.

(2) A second practical issue with flash memories drives is that a flash memory becomes unusable after a certain number of writes. As flash cells are stressed, they lose their ability to record and retain values. A typical limit is 1000,000 writes. Techniques for Prolonging the life

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of an SSD drive include front-ending the flash with a cache to delay and group write operation., using wear-leveling algorithms that evenly distribute writes across block of cells, and sophisticated badblock management techniques.

c

Ans (c) Read operation:-

Information is retrived from a CD or CD-ROM by a low-powered laser housed in an optical disk player, or drive unit. The laser shine through the clear polycarbonate while a motor spins the disk past it, The begining or end of a pit represent a 1; when no change in elevation occurs b/w intervals, a 0 is recorded.

eg. DVD.

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Write operation :-

Recall that on a magnetic disk information is recorded in concentric tracks. with the Simplest Constant angular velocity (CAV) System, the number of bits per track is constant

Q 4(a)

Ans (a) In example, Suppose 95% of the memory access are found in level 1. Then the average time to access a word can be expressed as

(0.95) (0.01 μs)+(0.05)(0.01 μs+0.1 μ

= 0.0095 + 0.0055

= 0.015 μs

The average access time is much closer to 0.01 μs than 0.1 μs as desired.

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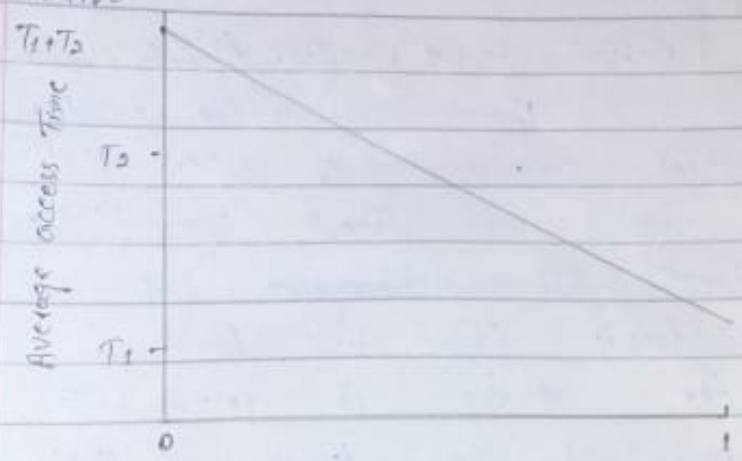
CURVE



Function of access involving only Level 1 (hit ratio)

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(b)

(b) Main memory address = 9F3A7Ch

In binary.

1001 1111 0011 1010 1110 1100

Tag	Set	word
1001 1110	0 1110 1011 1011	0 0

← 9 bits → ← 13 bits → ← 2 bits

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(a)

(d) So

7200 evaluation in 60sec

1 evaluation in 60/7200

1 revoluation in 6ms

1 revolution = covering one & entire track 500 sector

500 sector 6ms

1 Sector = 8 micro Second

Now there are two different things

(1) 2500 sectors So time = 2500 × 8ms = 20ms

(2) 1.28 Mb = 1342177.28 byte OR 2621.44 Sector = 26 Sectors = 20.976ms

Total time Case

Cas (1) 4+2+20 = 26 ms

Cas (2) 4+2+20.976 = 26.976 ms