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(Q.1)

"A"

1. The first to disable interrupts while an interrupt is being Processed. A disabled interrupt Simply means that processor can and will ignore that interrupt request Signals The drawback to the Precoding approach is that it does not take into account.
relative priority or time-critical needs.

2. A Second approach is to define priorities for interrupts and to allows an interrupts of higher priority interrupt handler to be itself interrupt.

"B"

The types of exchanges that are needy by indicating the major forms of input and output for modules are;

- **Memory to processor:**
  The processor reads an instruction or unit data from memory.
- **Processor to memory:-**
  The processor writes a unit data memory.
- **I/O to processor:**
  The processor read data from an I/O device
- **I/O to or from memory:**
  For these two case an I/O module is allowed to exchange data directly with memory without going through the processor using

direct memory access.

"C"

@ PI protocol Layer:

In this layer the packet is defined as the unit of transfer. one key function performed at this levels is a cache are consistent. A typical data packet payload is a block of data being sent to or from a Cache.

"D"

Physical and logical Architeture od pcie:

A root complex device also referred to as a chipset or a host bridge connects the processor and memory subsystem to the PCI Express switch fabric comprising one or more PCIe and PCIe Swith device.

- **Switch:** The Swith manages multiples PCIe Streams.
- **PCIe endpoint:**

An I/O device or controller that implements PCIe such as a Gigabit ethernet Swith, a graphics or Ucdio controller disk or Communication controller.

Allows older PCI devices to be Connected to PCIe-based Systems.

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(Q2)

(A) **Instruction cycle:**

The processing required for a single instruction is called an instruction cycle.

Using the simplified two-step description given previously the instruction cycle is depicted. Some of sort of unrecoverable error occurs, or a program instruction that halts the computer is encountered.

"B"

Instruction cycle state Diagram:

The instruction of state can cycle can be described as follows.

→ **(iac):** Determine the address of the previous of instruction usally this involes adding a fixed number to the address of the previous instruction.

→ **Instruction fetch:**

Read instruction from its memory location into the processor

→ **iod:** Analyze instruction to determine type of an operand in memory or availble via I/O then determine the address op of operand.

→ **operand fetch:** operand fetch from memory or read it in from I/O

→ **Data operation:** perform the operand indicated in the instruction. of them.

→ **operand stor:** write the result into memory or out to I/O

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"C"

Ans: Classes of interrupts:

1. program:

It is generated by some condition that occurs as a result of an instruction execution. Such as arithmetic overflow division by zero attempt to execute an illegal machine instruction access allowed or memory space.

ii Timer: It is generated by a timer within the processor This allows the operating system to perform certain are function on a regular basis.

iii :- I/O

iv :- ~~t/o~~ Hardware failure: It is generated by a failure. Such as power failure or memory parity error.

"D"

Ans

Bus Interconnection Scheme: The most common computer interconnection structures are based on the use of one or more system buses

(a) Data line: The data lines provide a path for moving data among system modules called data bus.

(b) Address lines: The address lines are used to designate the source or destination of data in data bus The width of the address bus determines the maximum possible memory of system

(c) control lines: The control lines are used to

to controll the accen to and the use of the data and address lines Because the data and and address lines are shared by all components.

Typicall control lines include:

Memory write, Memory read I/o write I/o read Transfer Ack, Bus request Bus grant interrupt request, interrupt Ack clock and Reset.

(Q3) "A"

Programming in Hardware:

The program hardware is in the form of hardware and is termed a hardwared program.

Suppose we construct a general-purpose configuration of arithmatic and logic fonctions. This set of a hardware will perform various function depending on control signals applied of the hardware.

Programming in Software:

The new method programming which is a sequence of codes or instruction is called Software programming.

"B"

Program flow of control without interrupt and With with interrupt:-

* In the interrupt cycles with processor check to see if any interrupts have occered indicated by the presence of an Interrupt signal.

* If no interrupts are pending the processor proceeds to the fetch cycle and fetches the next or instruction of the current program.

"C"

Disabled interrupt and nested interrupt processing

* A disable interrupt simply means that the processor can and will ignore that interrupts request signal. If an interrupt occurs during this time is generally remains pending and will be checked by the processor after the enable interrupts.
* A nested interrupt is to allow an interrupt to higher priority to cause a low priority interrupt occurs information is placed on the system stack and execution begins at t = 0. At t = 10 a printer interrupt. while the routine is still execing at t = 15 a Communication interrupts occurs.

(@ 4)

"A"

Memory (contents in hex): 300J; 301: 5940; 302

Step 1: 300J → IR; step 2: 3 → AC step 3: 5940 → IR; step 4: 3 + 2 = 5 → AC

Step 5: 7006 → IR; step 6: AC → Device

"B"

1 a. The PC contain 300, the address of the first instruction. This value is loaded in to the

2 bytes

transfer rate.

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MAR. b. The value in location 300 (which is the instruction with the value 1940 in hexadecimal) is loaded into the MBR. is loaded into the IR.

(2) a. address portion of the IR (940) is loaded into the MAR. b. The value in location is 940) is is loaded into (301) the MBR. and AC.

(3) a. The value in the PC (301) is loaded into the MAR b. The value in location 301 (which is the with is instruction with value (5941) is loaded into the MBR is loaded into the IR.

(4) a. The address portion of IR is (941) is loaded into the MAR. b. The valal in location (941) is loaded into the (MBR) c. The old value of the AC and the value of location MBR are added into the result Stored in the AC.

(5) a. The value in the PC (302) is loaded in to the MAR. b. The value in location 302 (which is the instruction with the value (2941) is loaded into the MBR. in IR.

(6) a The address portion of the IR (941) is loaded into the MAR b. The value in AC is loaded into the MBR. c. The value in the MBR is loaded Stored in in location (941).

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"C"

a. 2^{24} = 16MBytes

b. (1) If the local address bus is 32 bits the whole address can be transferred at once and decoded in memory however because the data bus is only 16 bits, it will require 2 cycles to fetch a 32 bit instruction or operand.

(2) The 16 bits of address placed address bus can't access the byte memory. this a more complex memory interface control is needed to latch the first part of the address and then the second part.

(c). The program counter must be at least 24 bits. Typically a 32 bit microprocessor will have a 32 bit external address bus and a 32-bit program counter inter onchip segment register are used that may work and now it will then it will have to be 8 bits long.

"D"

Ans:-

Clock cycle =

1 = 125 ns 8 MHz Bus cycle = 4 x 125 ns = 500 ns

2 bytes transferred every 500 ns, thus transfer rate.

4 MBytes/sec)

Doubling the frequency may mean adopting a new chip manufacturing technology (assuming each instructions will have the same number of clock cycles); doubling the external data bus mean wider (maybe never) on chip data bus drivers / latches and modifications to the bus control logic in the first case the speed of the memory chips will also need to double microprocessor in the second case the wordlength of the memory will have to double to be able to send/receive 32 bit quantities.

"E"

(a) During a single bus cycle, the 8-bit microprocessor transfers one byte while the 16-bit microprocessor transfer two bytes. The 16 bit microprocessor has twice the data transfer rate.

(b) Suppose we do 100 transfer two bytes operand and instruction of which 50 are one byte long and are two byte long. The 8 bit microprocessor takes $50 + (2 \times 16) - 50) = 150$ bus cycles for the transfer the 16-bit microprocessor require 50+50 bus cycles thus the data transfer rate differ by a factor of 1.5.

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"F"

A bus cycles takes 0.25 μs, so a memory cycles takes 1 μs. If both operands are even aligned it takes 2 μs to fetch the two operands. If one is odd-aligned the time required is 3 μs If both are odd-aligned the time required is 4 μs.

"G"

Consider a mix of 100 instructions and operands. On average, they consist of 20% 32 bit items 40% 16-bit items and 40% 8-bit The number of bus cycles required for the 16-bit microprocessor is (2×20)+40+40=120 for the 32-bit micro Processor the number required is 100. This amount to an improvement of 20/120 or about 17%.

The End

...11) is loaded).
... in AC is loaded
... the value in the MBR is loaded to
... location (941).