Assignment#1

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Ans#1

Data Processing

Data may take a wide variety of forms and the range of processing requirements is broad

Data Storage

The Computer performs a long-term data storage function. Files of data are stored onthe Computer for subse quent retrievel and update.

Data Movement

When data are moved over long dis tances to or form a remote device the process is known as data comm

Control

within the Computer a Control unit manages the Computer resources and orchestrates the performance of its functional part in response to instruction.

Ans#2

ISU (instruction sequence unit)

Determine the sequence in which instruction are executed in what is reffered to as a superscalar architecture.

IFU (instruction fetch unit):

Logic for fetching instruction

IDU (instruction decode unit)

The IDU is fed from the IFU buffers and is responsible for the parsing and decoding of all z/Architecture operation codes

LSU (load store unit)

it is responsible for handling all types of operand accesses of all length

XU (translation unit)

This unit translates logical address from instruction into physical address in main memory.

FXU (fixed point unit)

The Fxu executes fixed point arithematic operation

BFU (Binary floating point unit)

BFU handles all binary and hexadecimal floating point operation as well as fixed point multiplication operation

DFU (decimal floating point unit)

The DFU handles both fixed point and floating point operation on numbers that are stored as decimal digits.

RU (recovery unit)

The RU keeps a copy of the complete state of the system that includes all registers, collect hardware fault signals.

CoP (dedicated co-processor)

The CoP is responsible for data compression and encryption function for each core.

I-Cache

This is a 64-kB L1 instruction cache allowing the IFU to prefetch instruction before they are needed.

L2 Control

This is the control logic that manages the traffic through the two L2 caches

Data L2

A 1-MB L2 data cache for all memory traffic other than instruction

instr-L2

A1-MB L2 instruction cache

Ans#3

The IAS operates by respectively performing as instruction cycle. Each instruction cycle consist of two sub cycle

Fetch cycle

The opcode of next instruction is loaded into the IR and the address portion is loaded into the MAR. This instruction may be taken from the IBR or it can be obtained from memory by loading a word into the MBR and then down to the IBR, IR and MAR

Execute cycle

The control circuitry interprets the opcode & executes the instruction by sending out the appropriate control signals to cause data to be moved or an operation to be performed by the ALU.

Ans#4

No, These programs are never considered to be embedded because they are not an integral Component of a larger system

Ans#5

Yes, regardless of what the disk drive is used for. The software within the

disk driver controls the DHA hardware and is hard real time as well.

Ans#6

No, input-output drivers do not represent the embedded system.

Ans#7

Yes PDA is an embedded system becos it is just like a personal computer in hand

Ans#8

Yes the firmware inthe cellphone is control the radio hardware

Ans#9

if the FMS is not connected to the avionics and is used only for Logistics computerizations, a function readily performed on a ~~the~~ laptop then the FMS is clearly not embedded.

Ans#10

Yes, both inthe simulator and inthe thing being tested inthe HiL simulator Hardware is being controlled on both sides.

Ans#11

Yes. inthis case of system is the combination of the pacemaker and the person's heart.

Ans#12

Yes, it is part of a large system the engine and it is directly monitoring and controlling the engine through special hardware.

Ans#13

There are four main structural components.

CPU: Controls the operation of the comp and performs its data processing functions often simply referred to as processor

Main Memory: Store data

I/O: Moves data between the computer and its external environment.

System interconnection

Some mechanism that provides for Communication among CPU, main memory and i/o

Ans#14

The famous Moore's law which was propounded by Gordon Moore confounder of Intel, in 1965. Moore observed that the number of transistors that could be put on a single chip was doubling every year. The pace slowed to a doubling every 18 months in the 1970s but has sustained

that rate ever since.

The Concequences of Moor's Law are profound.

* The Cost of Computer Logic and memory circuitry has fallen at a dramatic rate.
* Because Logic and memory elements are placed closer together on more densely packed chips, the electrical path length is shortened, increasing operating speed.
* The Computer becomes smaller, making it more Convenient to place in a variety of environ
* There is a reduction in power requirements
* ~~There~~ with more circuitry on each chip there are fewer intechip

Ans#15

Computer Achitecture

Refers to those attributes of a system visible to a programmer or, put another way, those attributes that have a direct impact onth logical execution of a program

A term that is often used interchangeably with Computer aechitecture is instruction set architecture (ISA)

Computer organization.

Refer to the operational units and their interconnection that realize the architectural specification. Example of architectural attributes include the instruction set, the number of bits used to represent various data types etc.

Ans#16

* The current x86 offerings represent the result of decades of design effort on Complex instruction set computers (CISC). The x86 incorporates the sophisticated design principle once found only on mainframes and supercomputers and serves as an excellent exe of CISC design.
* An alternative approach to processor design is the reduced instruction set computer(RISC). The ARM architecture is used in a wide variety of embedded systems and is one of the most powerful and best designed RISC-based system on the market. In this section and the next we provide a brief overview of these two systems.

Ans#17

Microprocessor chips include registers and ALU and some part of control unit or instruction processing logic. As transistor density increased, it became possible to increase the complexity of the instruction set architecture and ultimately to add memory and more than one processor.

Ans#18

The Cortex-A and Cortex-A50 are app processors intended for mobile devices such as smartphones and e books readers as well as consumer devices such as digital TV and home gateways. These processors run at higher clock frequency and support a memory management unit(MMU) The Cortex-R is designed to support real time application, in which the timing of events needed to be controlled with rapid response to events. They can run at a fairly high clock frequency and have very low response latency. Cortex-M series have been developed primarily for the microcontroller domain where the need for fast, highly

Ans#19

(1) Here is a simple way to understand this problem. Contents are divided up into 5 bit instruction LH and RH

LH = 010FA

opcode = 01 ⇒ address = 0FA

RH = 216FB

opcode = 21

address = 0FB

LH

01 = 0000001 = LOAD M(x)

M(x) refers to the memory address location 0FA

The 1st five 5 bits of 0BA should read = LOAD M(0FA)

RH

21 = 0100001 = STOR M(x)

The seconds 5 bits of 0BA should read = STOR M(0FB)

Finally the assembly language code for 0BA 010FA210FB is

LOAD M(0FA)

STOR M(0FB)

(2) Contents are divided up into two 5 bit instruction LH and RH

LH = 010FA

opcode = 01

address = 0FA

RH = 0F08D

opcode = 0F

address = 08D

LH

01 = 00000001 = LOADM(x)

The first 5 bits of 08B should read = LOADM(0FA)

RH

0F = 00001111 = JUMP+M(x,0:19) refers memory address location 08D

The seconds bits of 08B should read = JUMP+M(08D,0:19)

Finally the assembly language code for 08B of 0FADF08D is

LOADM(0FA)

JUMPt M(08D,0:19)

(3) LH = 020FA

opcode = 02

address = 0FA

RH = 210FB

opcode = 21

address = 0FB

LH

02 = 00000010 = LOAD-M(x)

The first 5 bits of 08C should read
- LOAD-M(0FA)
RH
21 = 00100001 = STORM(X)
The secard 5 bits of 08C
should read - STORM(0FB)
Pinally the assembly language code for
08C 020FA210FB18
LOAD-M(0FA)
& STOR(0FB)

ANS20#

in 08A address the M(0FA) transfer to the accumulator and transfer contents of accumulator to memory location 0FB
in 08B address the M(0FA) transfer to the accumulator and take next instruction from Left half of M(08D)
In 0BC address the -M(0FA) transfer to the accumulator and transfer contents of accumulator to memory location 0FB.