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**Reg No. 16550**

**Mid term Assignment: No 3**

**Subject: Digital logic design**

**(Lab)**

**Instructor : Muhammad Amin**

### Lab: 3 Full Add

Observation Table:-

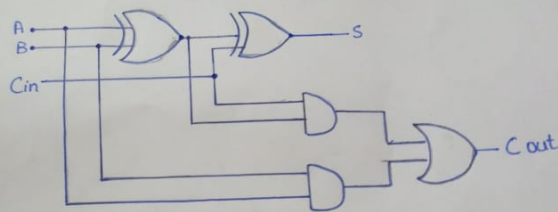
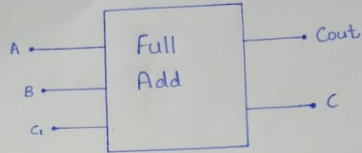


Table 3.1

Inputs			Outputs	
A	B	C <sub>i</sub>	Sum(S)	Carry(A <sub>v</sub> )
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1