Name # Kamran Khan

ID # 6990

Semester # 6th

Subject # VLSI Technology

Submitted to # Engr. Zulqarnain

Department # Electrical

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(Q No 1)

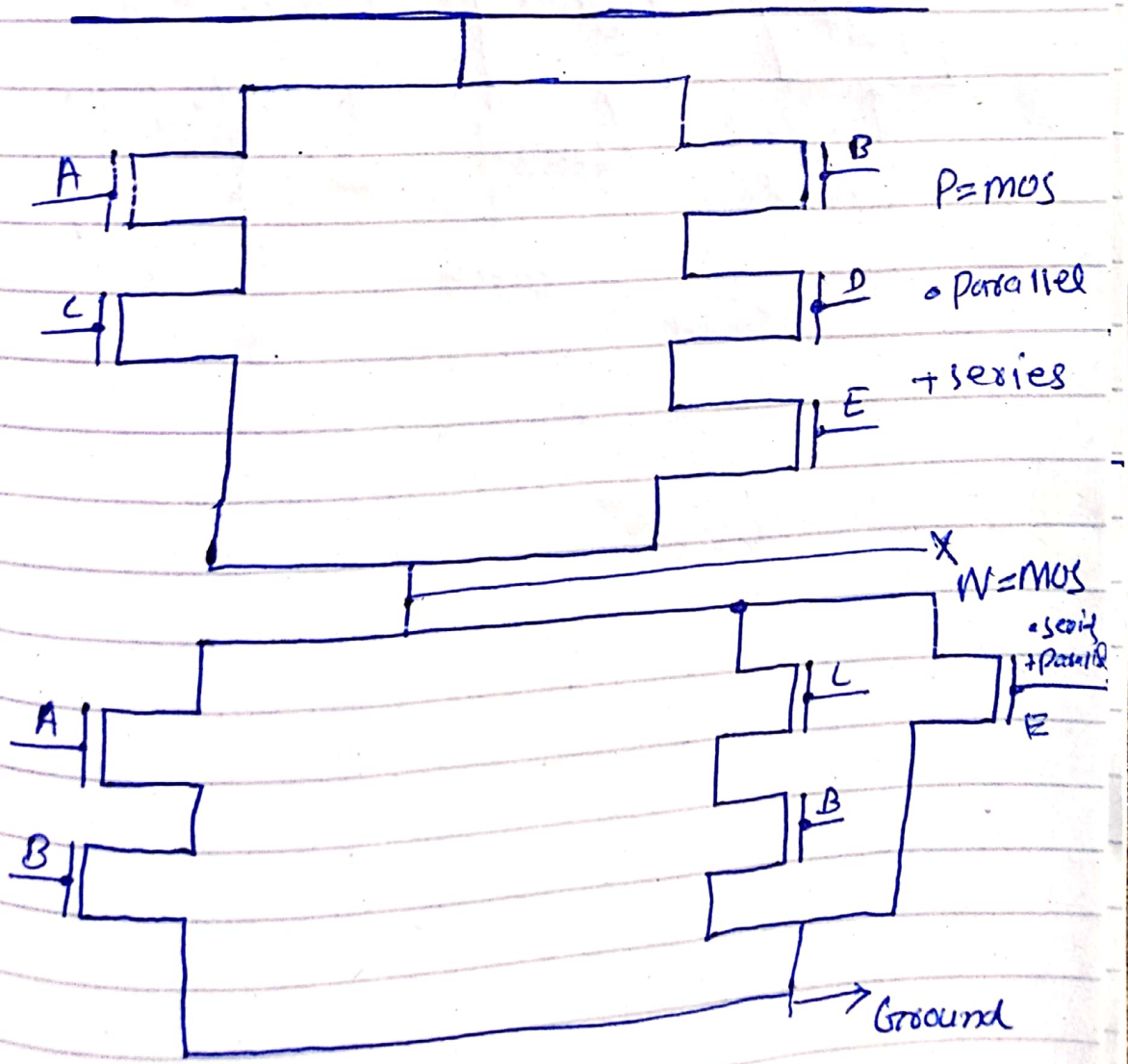
Design an area efficient layout for the cmos shown below

$F = AB + (C(D)E$

\# N = . Series
+ Parallel

P = . parallel
+ Series

$F = AB + C(.D)E$



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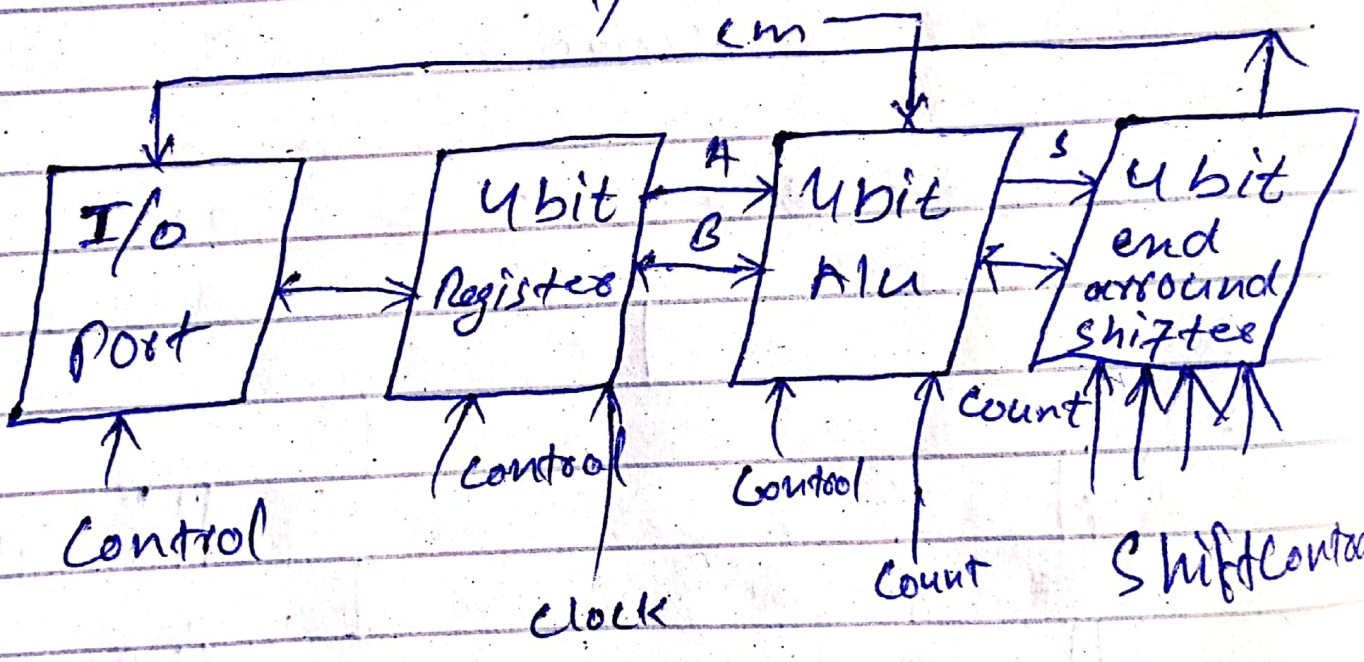
(pg 8) Kamran#ID 6990

(Q2) Give the subsystem design consideration of a four bit adder!

Ans!

Design consideration of a four bit adder!



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Design of 4-bit adder 1

Inputs		Outputs		
AK	BK	CK-1	SK	CK
0	0	0	0	0
0	0	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

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(Q No 3) b part

Any : Simple parity check code!

The simple parity-check code is the most familiar error-detecting code. in this code, a k-bit data word is changed to an n-bit code word where n=k+1. the extra bit, called the parity bit code is selected to make the total number OF 1s in the code word even. Although some implementation specify an odd number OF 1s. the minimum Hamming distance for this category is $d_{min}=2$, which means that the code is a single-bit error-detecting code and cannot correct any error.

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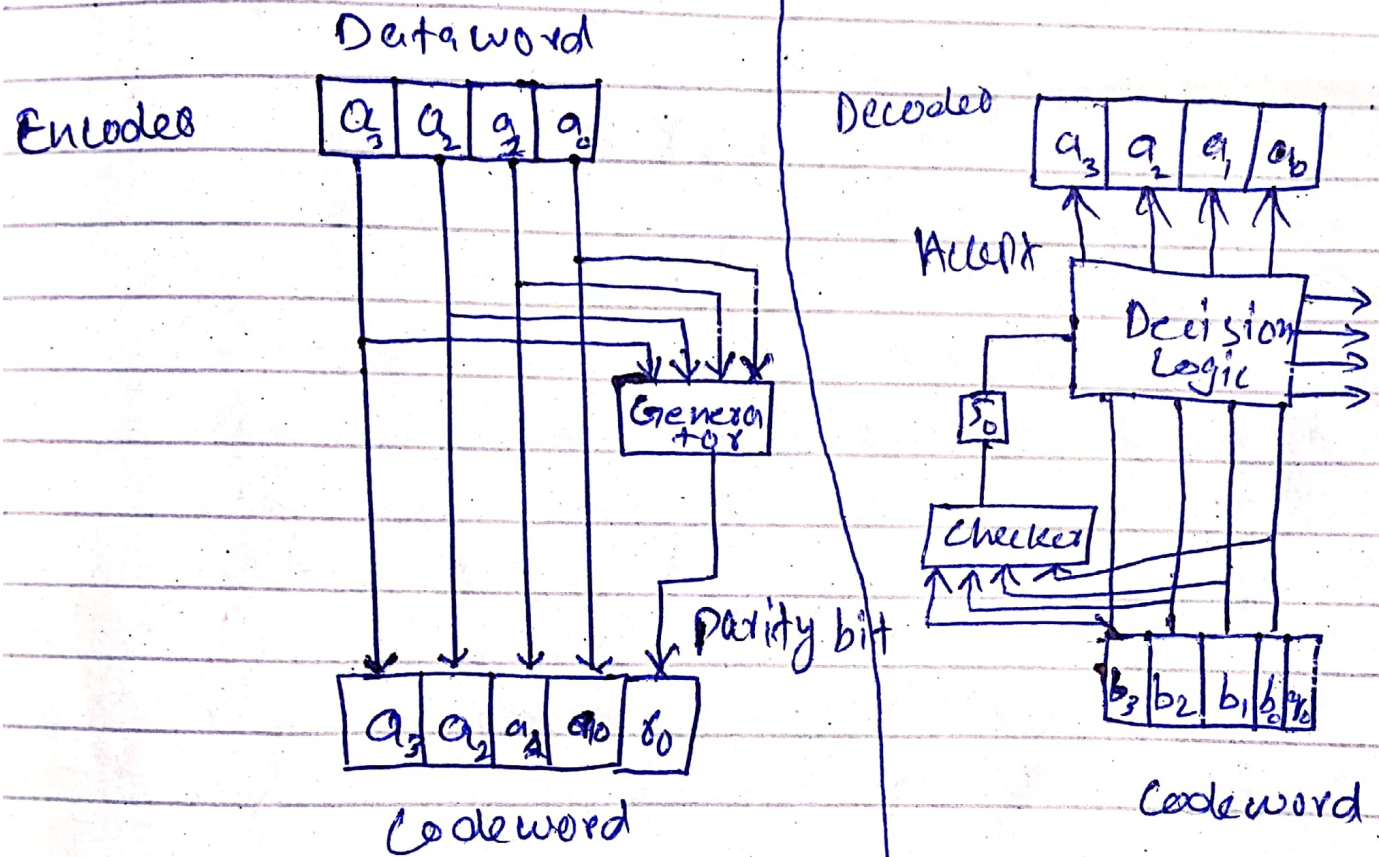
Simple parity check code diagram!



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(Ans) Q4) The Inverter have always Lower limit of the Power depends on the Sum of the threshold voltage of the nMOS and Vdd.

Logic function is Implemented by pull-down network only

Full swing output (VOL=GND and VOH = VDD)

Non-ratioed.

Faster switching speeds.

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(Q3 Part a)

(Ans!)

This is the particularly so in the case of the design of a VLSI system which could otherwise take so long as to send the whole system obsolete before it is OFF the drawing board.

But now some sensible concept applied in larger system design requirment.

Define the requirment properly & carefully.

partition the overall architecture into appropriate subsystem.

Consider communication path carefully in order to develop sensible interrelationships between system.

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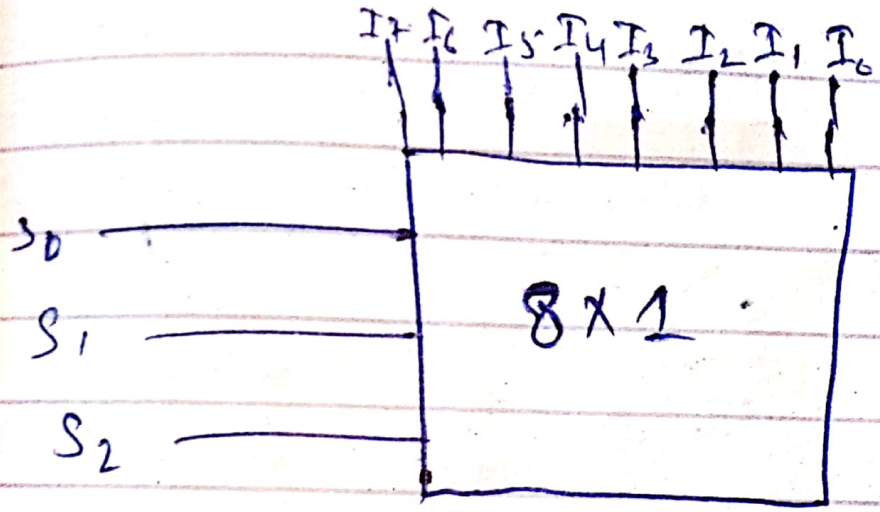
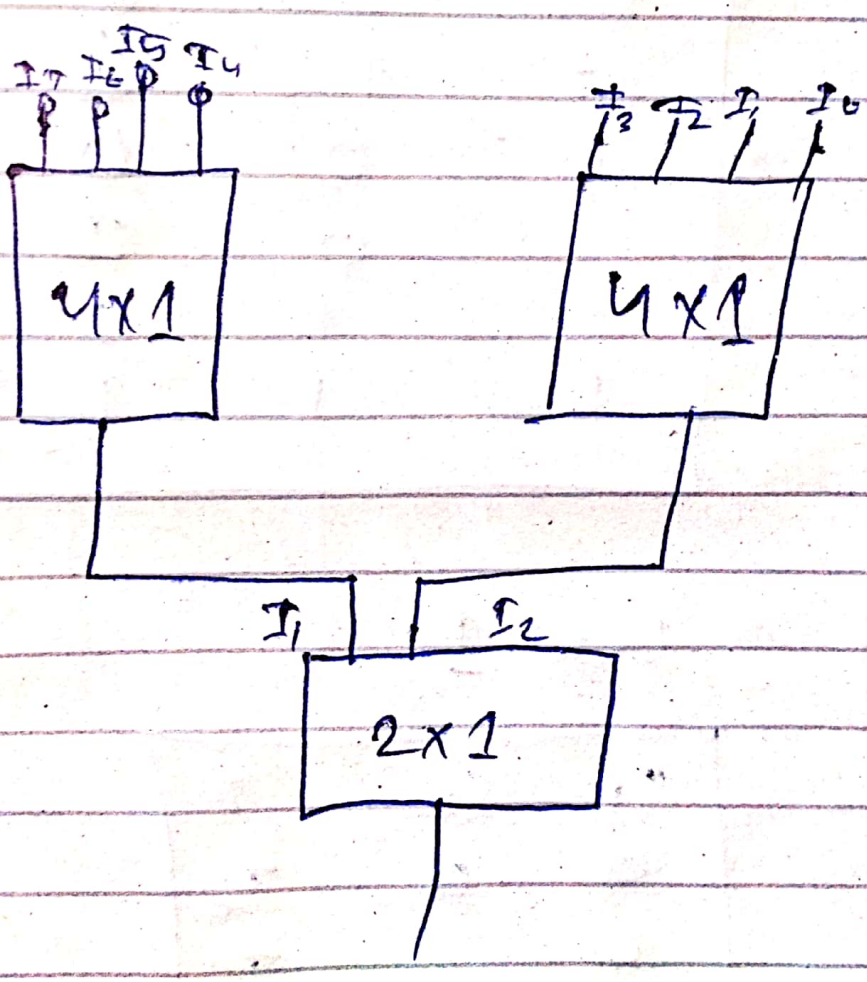
Kamran # (DH 6990

Q NO 5





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Truth table:

S_2	S_1	S_0	output
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

4 × 1

S_1	S_0	x
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

2 × 1

S_1	S_0	y
0	0	I_0
0	1	I_1

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8×1 mux By VD = Method

I_0	=	S_2	S_1	S_0
I_1	=	S_2	S_1	S_0
I_2	=	S_2	S_1	S_0
I_3	=	S_2	S_2	S_0
I_4	=	S_2	S_1	S_0
I_5	=	S_2	S_1	S_0
I_6	=	S_2	S_1	S_0
I_7	=	S_2	S_1	S_0

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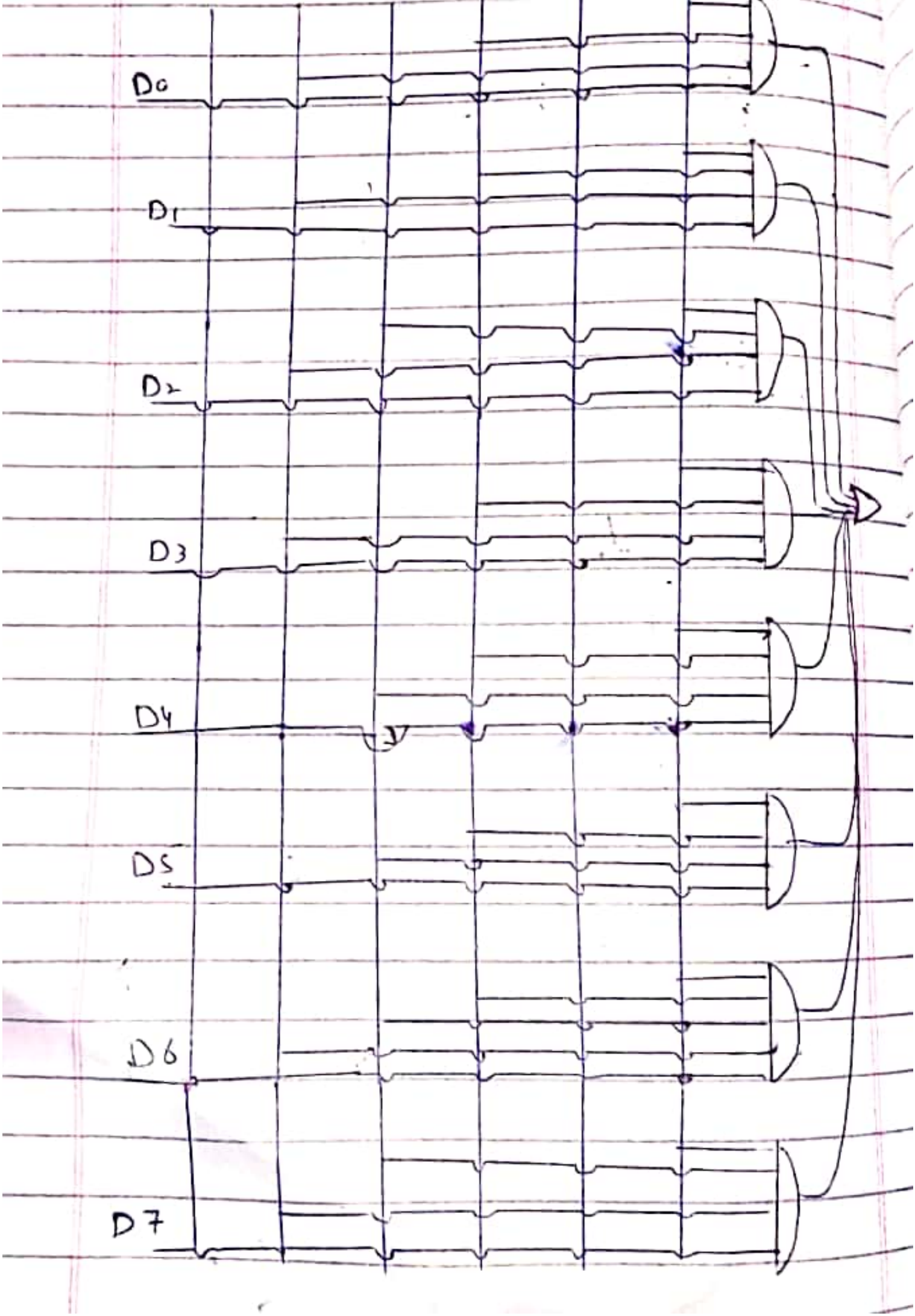

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