Q) What are the four main functions of a computer?

Computer operate through these four functions: input, output, processing, and storage.

INPUT: ~~The~~
The transfer of information into the system (e.g. through a keyboard).

OUTPUT:
The presentation of information to the user (e.g. on a screen).

PROCESSING:
The retrieval or manipulation of information into a new form (eg. results from a search engine).

STORAGE:
The storage of preservation of information for later use (e.g. files stored on a hard drive).

Draw the IBM z Enterprise EC12 Core layout and explain the function of each sub-area?

ISU (Instruction Sequence Unit):
Determines the sequence in which instructions are executed in what is referred to as a superscale architecture.

IFU (Instruction fetch Unit):
Logic for fetching instructions.

IDU (Instruction decode Unit):
The IDU is fed from the IFU buffers and is responsible for the parsing and decoding of all z/Architecture operation codes.

LSU (Load-store Unit):

It is responsible for handing all types of operand accesses of all lengths, modes and formats as defined in the Z/Architecture.

XU (Translation Unit):

This unit translates logical addresses from instructions into physical address in main memory. It contains TLB used to speed up memory access.

FXU (fixed Point Unit):

The FXU executes fixed-point arthmetic operations.

BFU (binary floating-Point unit):

The BFU handles all ~~bing~~ binary and hexadecimal floating-point operations, as well as fixed-point multiplications operations.

DFU (decimal floating-Point Unit):

The DFU handles both fixed-point and floating-point operations on numbers that are stored as decimal digits.

RU (recovery Unit) :

The RU keeps a copy of the complete state of the system that includes all registers, Collect hardware fault signals.

COP (dedicated Co-processor) :

The COP is responsible for data Compression and encryption functio for each core.

I-Cache :

This is a 64-KB L1 instruction Cache, allowing the IFU to prefet instructions before they are needed.

L2 Control :

This is the control logic that manage the traffic through the two L2 caches.

Data L2 :

A 1MB L2 data cache for all memory traffic other than ~~ist~~ instructions.

Instr L2 :

A 1MB L2 instruction cache.

B) Discuss the IAS operation in detail?

The IAS operats by prespectively performing an instruction cycle. Each instruction cycle Consist of two sub-cycles.

Fetch Cycle :

The opcode of next instruction is loaded into the IR and the address portion is loaded into the MAR. This instruction may be taken from the IBR, or it can be obtained from memory by ~~too~~ loading a word into the MBR, and then down to the IBR, IR and MAR.

Execute Cycle :

The control circuitry interprets the opcode and executes the instruction by sending out the appropvaite control signal to cause data to be moved or an operation to be performed by the ALU.

Q) Discuss the IAS operation using the flowchat is Figure 02

DATA TRANSFER :

Move data between memory and ALU registers or between two ALU registers.

UNCONDITIONAL BRANCH :

Normally, the control unit executes instructions is sequence from memory. This sequence can be changed by a branch instruction, which ~~facl~~ facilitates ~~repetive~~ repetitive operations.

CONDITIONAL BRANCH :

The branch can be made dependent on a condition, thus allowing decision point.

ARTHMETIC :

Operations performed by the ALU.

~~ADRESS~~ ADDRESS MODIFY :

Permits addresses to be computed in the ALU and then inserted into instructions sorted in memory. This allows a program considerable addressing flexibility.

Q) For each of the following examples, determine ~~we~~ whether this is an embedded system, explaining why or why not.

A) Are programs that understand physics and/or hardware embedded? For example, one that uses finite-element methods to predict fluid flow over airplane wings?

Ans) No. These programs are ~~very~~ never considered to be embedded because they are not an integral component of a larger system.

B) Is the internal microprocessor controlling a disk drive an example of an embedded system?

Ans) Yes, regardless of what the disk drive is used for. The software (filmware, actually) within the disk drive controls the HDA (head disk assembly) hardware and is hard real-time as well.

C) I/O drivers control hardware, So does the presence of an I/O driver imply that the computer executing the driver is embedded?

Ans) No, input-output drivers do not represent the embedded system.

E) Is the microprocessor controlling a cell phone an embedded system?

Ans) Yes, the firmware in the cell phone is controlling the radio hardware.

D) Is a PDA (Personal Digital Assistant) an embedded system?

Ans) Yes, a PDA is an embedded system.

F) Are the computer in a big phased-array radar considered embedded? These radars are 10-story buildings with one to three 100-foot diameter radiating patches on the sloped sides of the building.

Ans) Yes, these computers were generally some of the most powerful computers available when the system was built, are located in a large computer room occupying almost one whole floor of a building and may be hundreds of meters away from the radar hardware. However, the software running in these computer controls the radar

hardware; therefore, the computers are an integral component of a large system.

G) Is a traditional flight managment system (FMS) built into an airplane cockpit considered embedded?

Ans) If the FMS is not connected to the avionics and is used only for logistics computerization, a function readily performed on a laptop, then the FMS is clearly not embedded.

H) Are the computers in a hardware-in-the-loop (HIL) simulator embedded?

Ans) Yes, both in the simulator, and in the thing being tested in the HIL simulator. Hardware is being controlled on both sides.

I) Is the computer controlling a pacemaker in a person's chest an embedded computer?

Ans) Yes, in this case of the "system" is the combination of the pacemaker and the person's heart.

J) Is the Computer Controlling fuel injection in an automobile engine embedded?

Ans) Yes, it is part of a large System the engine, and it is directly monitoring and controlling the engine through ~~sep~~ special hardware.

following:

Main structural components of a Computer.

There are four main structural components.

CENTRAL PROCESSING UNIT (CPU):

Controls the operation of the computer and performs its data processing functions often simply referred to as processor.

MAIN MEMORY:

It stores data.

I/O:

Moves data between the computer and its external environment.

SYSTEM INTERCONNECTION:

Some mechanism that provides for communication among CPU, main memory and I/O.

B) Key characteristics of a planned computer family.

The characteristics of a family are as follows.

1) **Similar or Identical Instruction Set:**
In some cases, the lower end of ~~logic~~ the family has an ~~ist~~ instruction set that is a subset of that of the top end of the family. This means that programs can be moved up but not down.

2) **Similar or Identical Operating System:**
The some basic operating system is available for all family members.

3) **Increasing Speed:**
The rate of instruction execution increases from lower to higher family member.

4) **Increasing Number Of I/O Parts:**
The number of I/O parts increases in going from lower to higher family member.

5) **Increasing Memory Size :**
The size of main memory increases from lower to higher family members.

c) **Increasing Cost :**
At a given point in time, the cost of a system increases in going from lower to higher family members.

c) Stored Program Computer.
Storage of instructions in Computer memory to enable it to perform a variety of task in a sequence or intermittently. The idea was ~~intro~~ introduced in the Late 1940s by John von Neumann, who proposed that a program be electronically Stored in binary-number format in a memory device so that instruction Could be modified by the Computer as as determined by intermediate Computational results.

D) Moore's law ?

MOORE'S LAW :
The famous Moore's Law, which was pro found by ~~Gorden~~ Gorden Moore, Cofounder of intel in ~~19~~ 1965 [MOOR65]. Moore observed that the number of

transistors that could be put on a signal chip was doubling every year. The pace solved to a doubling every 18 months in the 1970s but has sustained that rate ever since.

The consequences of Moore's Law are profound.

1) The cost of computer logic and memory circuitry has fallen at a dramatic rate.
2) Because logic and memory elements are placed closer together or more densely packed chips, the electrical path length is shortened, increasing operating speed.
3) The computer becomes smaller, making it more convenient to place in a variety of environments.
4) There is a reduction in power requirments.
5) With more circuity on each chip there are fewer interchip connections.

E) Instruction cycle state diagram?

The States in instruction cycle can be discribed as follows.

Computer Organization and Computer architecture.

Computer Organization :

Computer Organization refers to the operational units and their interconnection that realize the architectural specifications. Examples of architectural attributes includes the instruction set, the number of bits used to represent various data types (e.g number, characters), I/O mechanisms and techniques for addressing memory.

Computer Architecture :

Computer architecture refers to those attributes of a system visible to a programmer or, put another way, those attributes that have a direct impact on the logical execution of a program.

RISC :

i) RISC stands for Reduced Instruction Set Computer.

ii) RISC processors have simple instructions taking about one clock cycle.

iii) Performance is optimized with more focus on software.

iv) It has no memory unit and uses separate hardware to implement instruction.

v) It is a hard-wired unit of programming.

vi) The most common RISC microprocessors are Alpha, ARC, ARM, AVR, PA-RISC and SPARC.

vii) RISC architecture is used in high-end applications such as video processing, telecommunications and image processing.

CISC :

i) CISC stands for Complex Instruction set Computer.

ii) CISC processor has complex instruction that takes up multiple clocks for execution.

iii) Performance is optimized with more

focus on hardware.

iv) It has a memory unit to implement complex instruction.

v) It has a microprogramming unit.

vi) Examples of CISC processors are the System/360, VAX, PDP-11, Motorola 68000 family and intel x86 CPUs.

vii) CISC architecture is used in low-end applications such as security system, home automation etc.

c) Microprocessors and Microcontrollers.

MICROPROCESSORS :

Microprocessor ~~chips~~ Chips include registers, an ALU, and some sort of control unit or instruction processing logic. As transistor density increased, it become possible to increase the complexity of the instruction set architecture, and ultimately to add memory and more than one processor.

MICROCONTROLLER :

A microcontroller is a single chip that contains that processor, non-volatile memory for the program (ROM), volatile memory for input and out (RAM), a clock and an

I/o control unit. The processor portion of the microcontroller has a much lower Silicon area than other microprocessors and much higher energy efficiency.

D) Cortex-A, Cortex-R, and Cortex-M.

Cortex-A :

The Cortex-A is application processor, intended for mobile devices such as Smartphones and eBook readers, as well as Consumer devices such as digital TV and have gateways (e.g DSL and Cable internet modems) These processors runs at higher Clock frequency (over 1 GHz) and support a memory managment unit (MMU).

Cortex-R :

The Cortex-R is designed to support real-time applications, in which the timming of events needs to be Controlled with rapid response to events. They can run at a fairly high clock ~~freqe~~ frequency (e.g 200MHz to 800MHz) and have very low response latency.

Cortex-M :

The Cortex-M Series processors have been developed primarily for the microcontroller domain where the need for fast, highly deterministic interrupt managment is coupled with the desire for extremly low gate count and lowest possible power consumption.

A) Given the memory contents of the IAS Computer shown below.

Address	Contents
08A	010FA210FB
08B	010FA0F08D
08C	020FA210FB

a) shown the assembly language code for the program, starting at address 08A.

(1) Here is a simple way to understand this problem.
Contents are divided up into two 5 bit instructions, LH and RH.

LH instruction = 010FA
op code = 01
address = 0FA
RH instruction = 210FB
opcode = 21
address = 0FB

Since this is in hexadecimal form you have to convert the number to binary form:

LH instruction:
01 = 0000001 = LOAD M(X)
The first 5 bits of 08A
Should read - LOAD M(0FA)

RH instruction:

21 = 00100001 = STOR M(x)

The second 5 bits of 0BA should read - STOR M(0FB)

Finally the assembly language code for 0BA 010FA210FB is

LOAD M(0FA)

STOR (0FB)

2) Here is a simple way to understand this problem.

Contents are divided up into two 5 bit instructions, LH and RH.

LH instruction = 010FA

opcode = 01

address = 0FA

RH instruction = 0F08D

opcode = 0F

address = 08D

Since this is a hexadecimal form you have to convert numbers to binary form;

LH instruction:

01 = 00000001 = LOAD M(x)

M(x) refers to the memory address location 0FA

The first 5 bits of 08B should read - LOAD M(0FA)
RH instruction :
0F = 00001111 = JUMP + M (X, 0:19)
refers to the memory address location 08D
The second 5 bits of 08D should read - JUMP + M (08D, 0:19)

Finally the assembly language code for 08B 010FA0F08D is
LOAD M(0FA)
JUMP + M (08D, 0:19)

3) Here is a simple way to understand this ;
Content are divided up into two 5 bit instructions, LH and RH

LH instruction = 020 FA
OPcode = 02
address = 0FA

RH instruction = 210FB
OPcode = 21
address = 0FB

Since this is in hexadecimal form, you have to convert the numbers to binary form;
(use the IAS instruction Set)

LH instruction:
02 = 00000010 = LOAD-M(X)
The first 5 bits of 08C
Should read - LOAD - M (0FA)

RH instruction:
21 = 00100001 = STOR M(X)
The second 5 bits of 08C
Should read - STOR M(0FB)

Finally the assembly language code for 08C 020FA210FB is
LOAD - M (0FA)
STOR M1 (0FB)

b) Explain what is program does.

1) In 08A address, the M (0FA) transfer to the accumulator and transfer contents of accumulator to memory location 0FB.

2) In 08B, the M (0FA) transfer to the accumulator and take next instruction from left half of M (08D)

3) In 08C address, the M (0FA) transfer to the accumulator and transfer contents of accumulator to memory location 0FB.

B) On the IAS, what would the machine code instruction look ---- How many ---- during the instruction cycle?

(a) opcode = 00000001
operand = 000000000010

(b) In, the beginning, the CPU have to fetch the instruction from the memory, Then the instruction will include the address of the data which is required to load. Through the execution time, the memory will be accessed in that time to load the data contents which is located at that address for a total of two trips to memory.

Q) In Figure 03, indicate the width, in bits, of each data path (e.g between AC and ALU).

Ans)
- Overall data paths to/from MBR is 40 bits.
- overall data paths to/from MAR is 12 bits.
- All paths to/from AC is 40 bits.
- All paths to/from MQ is 40 bits.