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Assignment: **Computer Architecture**

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Q No.01:

Answer: **Function of each sub area:-**

ISU (Instruction sequence Unit):

Determine the sequence in which instructions are executed in what is referred to as a superscalar architecture.

IFU (Instruction Fetch Unit):

Logic for fetching instructions.

IDU (Instruction Decode Unit):

The IDU is fed from the IFU buffers, and is responsible for the parsing and decoding of all Z/ architecture operating codes.

LSU (Load-Store Unit):

It is responsible for handling all types of operand accessories of all length, nodes and formats as defined in the Z/Architecture.

XU (Translation Unit):

This unit translate logical addresses from instructions into physical addresses in main memories.

FXU (Fixed Point Unit):

The FXO executes fixed points arithmetic operations.

BFU (Binary Floating Point Unit):

The BFU handles all binary and hexadecimal floating point operation as well as fixed point multiplication.

DFU (Decimal Floating Point Unit):

The DFU handles both fixed point and floating operation on numbers that are stored as decimal digits.

RU (Recovery Unit):

The RU keeps a copy of the complete state of the system that includes all registers, collects hardware fault, signals etc.

COP (Dedicated Co-Processor):

The COP is responsible for the data compression and encryption function for each core.

I-Cache:

This is a 64-KB L1 instruction cache, allowing IFU to prefetch instruction before they are needed.

L2 Control:

This is a control logic that manages the traffic through the two L2 cache.

Data-L2:

A 1-MB L2 data cache for all memory traffic other than instructions.

Instr-L2:

A 1-MB L2 instruction cache.

Answer (B):

IAS Operation:-

The IAS operates by repetitive performing an instruction cycle. Each instruction cycle consists of two sub cycles.

1. **Fetch Cycle:**

   During fetch cycle, the opcode of the next instruction is loaded into the IR and the address portion is loaded into MAR. This instruction may be taken from the IBR, or it can be obtained from memory by loading a word into the MBR, and then down to the IBR, IR and MAR.

2. **Execute Cycle:**

   Control circuiting interprets the opcode and executes the instruction by sending out the appropriate control signals to cause data to be moved or an operation to be performed by the ALU.

Answer (C):

Embedded System:

The term embedded system refers to the use electronics and software within a product as opposed to a general purpose computer, such as laptop or desktop system. Today, many devices that use electric power have an embedded computing system.

Different embedded systems used in everyday life are;

Cell phones, digital cameras, video camera, calculators, microwave ovens, home security systems, washing machines, lightning systems, printer etc.

Answer (D):

Different desktop applications that require the great power of contemprory microprocessor based system are;

- Image processing
- Three dimensional rendering
- Speed recognition
- Video conferencing
- Multimedia authority
- Voice and video connection of files
- Simulation modelling

Answer (E):

The techniques used in contemporary processors to increase speed are following:

- **Pipelining:**

  Pipelining enables a processor to work simultaneously on multiple instructions by performing a different phase for each of the multiple instructions at the same time.
- **Branch Prediction:**

  Branch prediction potentially increases the amount of work available for the process to execute.
- **Superscalar Executing:**

  This is the ability to issue more than one instruction in every processor clock cycle. In effect, multiple parallel pipelines are used.
- **Data flow analysis:**

  The processor analyse which instruction as are dependent on each other's result, or data to create an optimized schedule of instruction.
- **Speculative Execution:**

  This enables the processor to keep its execution engine as busy as possible by executing instructions that are likely to be needed.

Answer (F):

The problem created due to increase in clock speed and logic densities of the processor are;

- **Power:**

  As the density of logic and the clock spped on a chip increase, so does the power density. The difficulty of dissipating the heat generated on high density, high speed chip is becoming a serious design issue.
- **RC delay:**

  The speed at which electrons can flow on a chipbetween transistor is limited by the resistence and capicitoence of the metal wires connecting them. Specifically, delay increase as the RC product increase.
- **Memory Latency and throughput:**

  Memory access speed (latency) and transfor speed (throughput) lay processor speeds.

Answer (G):

Consider a program running on a single processor which that a function (1-f) of the execution time includes code that is inherently sequential, and a function f that involves codes that is infinitly parallilizable with no scheduling overhead.

Let T be the total execution time of the program using a single processor. Then the speedup wing a parallel processor with N processors that fully exploits the parallel portion of the programme is as follow;

Speedup= Time to execute programme on a single processor/time to execute programme on N parallel processing

Speedup= T (1-f) + Tf/ T(1-f)+ Tf/N = 1/ (1-f) + f/N

Answer (H):

The use of multiple processors on the same chip, also referred to as multiple core or multicore. Provides the potential to increase performance without increasing the clock rate. If the software can support the effective use of multiple processors. Then doubling the number of processors almost double performance. Two core chips were quickly followed by four-core chips, then 8, then 16 and so on.

MIC:

The leap in performance as well the challenges in developing software to exploit such a large number of cores has led to the introduction of new term called many integrated core (MIC). The multicore and MIC strategy involves a homogenous collection of general purpose processors on a single chip.

GPU: (GPGPU)

A GPU is a core designed to perform parallel operations on graphics data. It is found on a plug-in graphics cord. It is used to encode and rendered 2D and 3D graphics as well as process video. GPU perform parallel operations on multiple sets of data, they are increasingly being used as vector processors for a variety of applications that require repetitive computations.

Answer (I):

QuickPath Interconnect (QPI) Protocol layer:-

- In this layer, the packet is defined as the unit of transfer.
- The packet contents definition is standardized with same flexibility allowed to meet differing market segment requirments
- One key function performed at this layer is a cache coherency protocol, which deals with making sure that main memory valves held in multiple caches are consistent.

Answer (J):

Physical and Logical Architicture of PCIe:

Root Complex:

- It is also called "chipset" or "a host bridge", which connects the processors and memory subsystem to the PCI express switch febric comprising one or more PCIe and PCIe switch devices.
- The root complex act as a buffering device to deal with difference in data rates between I/0 controllers and memory and processing components.
- PCIe links from the chipset many attach to the following kinds of devices that implements PCIe.

Switch:

The switch manages multiple PCIe stream.

PCIe endpoint:

An I/0 device or controller that implement PCIe. Such as gigabit Ethernet switch, a graphics, disk interface etc.

Legacy Endpoint:

Legacy endpoint category is intended for existing designs that have been migrated to PCI express, and it allow legacy behaviours such as use of I/0 space and locked transaction.

PCIe / PCI bridge:

Allows older PCI devices to be connected to the PCIe-based syatem.

Q2:
Answer (A):

Structural Components of Computer:-

There are four main structural components of computer.

- **Central Processing Unit (CPU):**

It control the operation of the computer and performs its data processing functions; often simply reffered to as “processor”.

- **Main Memory:**

It stored data.

- **I/O:**

It moves data between the computer and its external environment.

- **System interconnection:**

Some mechanism that provides for communication among CPU, main memory and I/O. A common example of system interconnection is by means of a “system bus”.

Answer (B):

The characteristic of computer family are as follows:

- **Similar or identical instruction sets:**

In some cases the lower end of the family has an instruction set that is a subset of that of the top end of the family. This means that program can move up but not down.

- **Similar or identical operating system:**

The some basic operating system is available for all family members.

- **Increasing Speed:**

The rate of instruction execution increase in going from lower to higher family members.

- **Increasing number of I/O parts:**

The number of I/O parts increase in going from lower to higher family member.

- **Increasing memory size:**

The size of main memory increase going from lower to higher family members.

- **Increase Cost:**

At a given point in time, the cost of a system increases in going from lower to higher family members.

Answer (C):

- **Stored Programme Computer:-**

A fundamental design approach first implemented in the first IAS computer is known as the "stored-programme concept". This idea is usually attributed to the mathematician John Van Neumann. The first publication of the idea was in 1945 proposal by Van Neumann for a new computer, the EDVAC (Electronic Discrete Variable Computer).

In 1946, Van Neumann and his colleagues began the design of a new stored-programme computer, reffered to as the "IAS Computer" of the Princeton Institute for Advanced Studies. It consists of;

I. A main memory, which stores both data and instructions.
II. An arithmetic and logic unit (ALU), Capable of operating on binary data.

Answer (D):

- **Moore's Law:-**

The famous Moore's law, which was proposed by Gorden Moore, co-founder of Intel, in 1965. Moore observed that the number of transistors that could be put on a single chip was doubling every year, and correctly predicted that the pace would be continue in the near future.

The consequences of the Moore's law are;

- The cost of computer logic and memory circuitry has fallen at a dramatic rate.
- The computer becomes smaller, making it more convenient to place in a variety of environments.
- There is a reduction in power requirements.

- The interconnection on the integrated circuit are much more reliable than solder connection.

Answer (E):

- **Instruction Cycle State Diagram:-**

The states in instruction cycle state diagram are follows;

- **Instruction address calculation (IAC):**

  Determine the address of the next instruction to be executed. Usually this involves adding a fixed number to the address of the previous instruction.

- **Instruction Fetch (IF):**

  Read instruction from its memory into the processor.

- **Instruction Operating Decoding (IOD):**

  Analyse instruction to determine type of operation to be performed and operand(s) to be used.

- **Operand Address Calculation (OAC):**

  If the operation involves reference to an operand in memory or available via I/O, then determine the address of the operand.

- **Operand Fetch (OF):**

  Fetch the operand from memory or read it in the form of I/O.

- **Data Operand (DO):**

  Perform the operation indicated in the instruction.

- **Operand Store (OS):**

  Write the result into memory or out to I/O.

Answer (F):

Classes of Interrupts:-

- **Program:**

It is generated by some condition that occurs as a result of an instruction execution, such as arithmetic overflow, division by zero, attempt to execute an illegal machine instruction or reference outside a user's allowed memory space.

- **Timer:**

It is generated by a timer within the processor. This allows the operating system to perform certain function on a regular basis.

- **I/O:**

It is generated by an I/O controller, to signal normal completion of an operation, request service from the processor or to signal or verify of error conditions.

- **Hardware failure:**

It is generated by a failure such as power failure or memory failure error.

Answer (G):

Bus Interconnection Scheme:-

The most common computer interconnection structures are based on the use of one or more system buses.

A system bus consists typically of about fifty to hundreds of separate lines. The lines can be classified into their functional groups, data, address and control lines.

- **Data Lines:**

The data line provides a path for moving data among system modules. These lines are collectively called the "data bus". The data bus may consist of 32, 64, 128 or even more separate lines. The number of lines being referred to as "width of data bus".

- **Address Lines:**

The address lines are used to designate the source or destination of the data on the data bus. The width of the address bus determines the maximum possible memory capacity of the system.

- **Control Lines:**

The control lines are used to control the access to and the use of the data and address lines. Because the data and the address lines are shared by all components, there must be a means of controlling their use. Typical control lines include; Memory circuit, memory read, I/O write, I/O read, reset etc.'

Q3:

Answer (A):

- **Computer Architecture:-**

Computer Architecture refers to the attribute of a system visible to a programmer or put another way, these attributes that have a direct impact on the logical execution of a programme. A trend that is often used interchangeably with computer architecture is "instruction set architecture (ISA).

- **Computer Organization:**

Computer Organization refers to the operational units and their interconnections that realize the architecture specifications. Examples of architecture attributes includes the instruction set, the number of bits used to represent various data types (e.g. numbers, characters). I/O mechanism and techniques for addressing memory.

Answer (B):

- **CISC:**

The current x86 represent the result of decodes of design effort on "complex instruction set computer (CISCs)".

The x86 incorporates the sophisticated design principles once found only on mainframes and super –computers and sever as an excellent example of CISC design.

- **RISC:**

An alternative approach to processor design is the “reduced instruction set computer (RISC).

The ARM architecture is used in a wide variety of embedded systems and is one of the mass powerful and best-designed RISC- based systems on the market. In this section and the next section, we provide a brief overview of these two systems.

Answer (C):

- **Microprocessor:**

A microprocessor chips included registers, an ALU and some sort of control unit or instruction processing logic. As transistor density increased it become possible to increase the complexity of the instruction set architecture and ultimately to add memory and more than one processor. Micro-processor chips, includes multiple cores and substantial amount cache memory.

- **Microcontroller:**

A microcontroller is a single chip that contains the processor, non-volatile memory for the programme (ROM), volatile memory for input and output (RAM), a clock and an I/O control unit. The processor portion of the microcontroller has a much lower silicon area than other microprocessors and much higher energy.

Ans (D):

- **Cortex-A:**

The cortex-A and cortex-A50 are application processors, intended for mobile device such as smart-Phones and eBook readers, as well as consumer devices such as digital TV and home gateways (e.g DSL and cable internal modems). These processors ran at higher clock frequency and support a memory management unit (MMU).

- **Cortex-R:**

The cortex-R is designed to support real-time applications in which the timing of events needs to be controlled with rapid response to events. They can ran at a fairly high clock frequency and have very low response latency.

- **Cortex-M:**

Cortex-M series processors have been developed primarily for the microcontroller domain where the need for fast, highly deterministic interrupt management to coupled with the desire for extremely low gate count and lowest possible power consumption.

Answer (E):

- In the interrupt cycle, the processors checks to see if any interrupts have occurred, indicated by the presence of an interrupt signal.
- If no interrupts are pending, the processor proceeds to the fetch cycle and fetch cycle and fetches the next interruption of the current programme.

Answer (F):

- **Disabled Interrupt:**

A disabled interrupt simply means that the processer can and will ignore that interrupt request signal. If an interrupt occurs during this time .it generally rerraing pending and will be checked by the processor after the processor has enabled interrupts when a user program is executing and an interrupt occurs interrupts are disabled immediately

- **Nested interrupt :**

Nested interrupt is to allow interrupt of higher priority to cause a lower priority interrupt handler to be itself interrupted. A user program begins at t=0. At t=10, a printed interrupt occurs user information is placed on the system stack and execution continues at the printer “interrupts service routine” (ISR). While this routine is still executing at t = 15, a communication interrupt occurs.

Answer (G):

- **Programming in Hardware:**

The program is in the form of hardware and in termed as “hardware program”. Suppose we construct a general purpose configuration of arithmetic and logic function. This set of hardware will perform various functions on data defending on control signal applied to the hardware. In the original case of customized hardware, the system accepts data and producers result.

- **Programming in software:**

The new method of performing which is a sequence of codes or instruction is called software programming.

In this method, programming is much easier instead of rewiring the hardware for each new program. All we need to do is provide a new sequence of codes. Each codes is in effect, an instruments and part of the hardware interrupts each instruction and generates control signals.

Q4:

Answer (A):

- ***1.*** Here is a simple way to understand this problem
- Contents are divided up into two bits instructions, LH and RH

  LH instruction = 010FA
  Opcode = 01
  Address = OFA
  RH instruction = 210 FB
  Opcode = z1
  Address = OFB
  Since this in hexadecimal form, you have to convert this numbers to binary form.
- **LH Instruction:**

01 = 00000001 = LOAD M (X)

M (X) refers to the memory address location OFA

The first 5bits of 08A should read – Load M (OFA)

- **RH Instruction:**

Z1 = 00100001 = STOR M (X)

M (X) refers to the memory address location OFB

The second 5bits of O&A should read – STOR M (OFB)

Finally the assembly language code for O&A 010FAZ10FB is

LOAD M (OFA)

STOR M (OFB)

- ***2.*** Here is a simple way to understand this problem.
- Contents are divided up into two 5bit instruction, LH and RH

LH instruction = 010FA

Opcode = 01

Address = OFA

RH instruction = OFO&D

Opcode = OF

Address = O&D

Now convert this number into binary function form;

- **LH instruction:**

  01 = 00000001 = LOAD M (X)

  M (X) refers to memory address location OFA

  The first 5bits of O&B should read – LOAD M (OFA)

- **RH Instruction:**

  OF = 00001111 = JUMP + M (X, 0 = 19) refers to memory address location O&D

  The second 5bits of O&B should read – JUMP + M (O&D, 0 = 19)

  Finally the assembly language codes for O&B 010FAOFO&D is;

  LOAD M (OFA)

JUMP + M () & D, 0 = 19)

- ***3.*** Here is a simple way to understand this problem;

Contents are divided upto two 5bits instruction, LH and RH

LH instruction = 020FA

Opcode = 02

Address = OFA

RH instruction = 210FB

Opcode = 21

Address = OFB

Since this is in hexadecimal form, you have to convert the numbers to binary form.

- **LH Instruction:**

02 = 000000010 = LOAD – M (X)

M (X) refers to the memory address location OFA

The first 5bits of O& C should read – LOAD – M (OFA)

- **RH Instruction:**

21 = 00100001 = STOR M (X)

M (X) refers to the memory address location OFB

The second 5bits of O&C should read – STOR M (OFB)

Finally the assembly language code for O & C 020FA210FB is

LOAD – M (OFA)

STOR – M (OFB)

Answer (B):

1. In O&A address, the M (OFA) transfer to the accumulation and transfer contents of accumulator to memory location OFB.
2. In O&B address, the M (OFA) transfer to the accumulator and take next instruction from left half of M (O&D).
3. In O&C address, the M (OFA) transfer to the accumulator and transfer contents of accumulators to memory location OFB.

Answer (C):

- **Effective CPI:**

CPI = (1 * 46000) + (2 * 33000) + (2 * 16000) + (2 * 9000) / 100

CPI = 162000/100

CPI = 1620

- **MIPS Rate:**

MIPS rate = 60 MHz / 1620 * 10^6

MIPS rate = 60 * 10^6 Hz / 1620 * 10^6

MIPS rate = 60 Hz / 1620

MIPS rate = 0.037

- **Executive Time:**

T = Ic / (MIPS * 10^6)

T = 104000 / (0.037 * 10^6)

T = 104000 / 37 * 10^3

T = 2811 *10 -^{3}

T = 2.811 Sec

Answer (D):

(a) : Since we have the same instruction mix, that means the additional instructions for each task could be allocated appropriately between the instruction types. Therefore, the following table be gotten:

Instruction	***CPI***	***Instruction Mix***
Arithmetic and Logic	1	60%
Load/Store with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	12	10%

The average CPI = (1 * 0.6) + (2 * 0.18) + (1 * 0.12) + (12 * 0.1)
CPI = 2.64
Therefore , the CPI has been increased since the time for memory access is also increased.

(b) MPI = 400 / 2.64 = 152

There is a corresponding drop in the MIPS rate.

(c) The speed up factor equal to the ratio of the execution times.

The execution time iscalculated as the follwing:

$T = Ic / (MIPS * 10^6)$

For one processor, $T1 = (2 * 20^6) / (178 * 10^6)$

T1 = 11 ms

Answer (F):

(a) 224 = 16 Mbytes

(b) (1) if the local address bus is 32 bites, the whole address can betransferred at once and decoded in memory. However, because the data bus is only 16 bits, it will requires 2 cycles to fetch a 32 bit instruction or operand.

(c) The 16-bits of the address placed on the address bus cannot access the whole memory. Thus a more complex memory interface control need to fetch the first part of the address and then the second part.

(d) The program counter must be at least 24 bits. Typically, a 32 bits microprocessor will have a 32 bits external address bus and a 32 bit program counterm unless onchip segment register are used that may work with smaller program counter. If the instruction register is to contain the whole instruction it will have to be 32-bit long; if it qill contain only the OP code (called the OP code register) then it will here to be 8 bits long.

Answer (G):

A bus cycle takes 0.25 us, so a memory cycle takes 1us. If both operands are even aligned, it takes 2us to fetch the two operands. If one is odd aligned, the time required is zero. If both are odd aligned, the time required is 4us.

[{(THE END)}]