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Semmester : (06)

Assignment : (01)

Subjeetect : VLSI

INStructor : Engr Zulqarnain

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Ans I

Depletion Load N-MOS

In integrated Circuits depletion - load NMOS is a form of digital logic family that uses only a single power supply voltage, unlike earlier nMOS Logic families that needed more than one different power Supply voltage.

* Channels implant to adjust the threshold voltage

* **Advantages:**

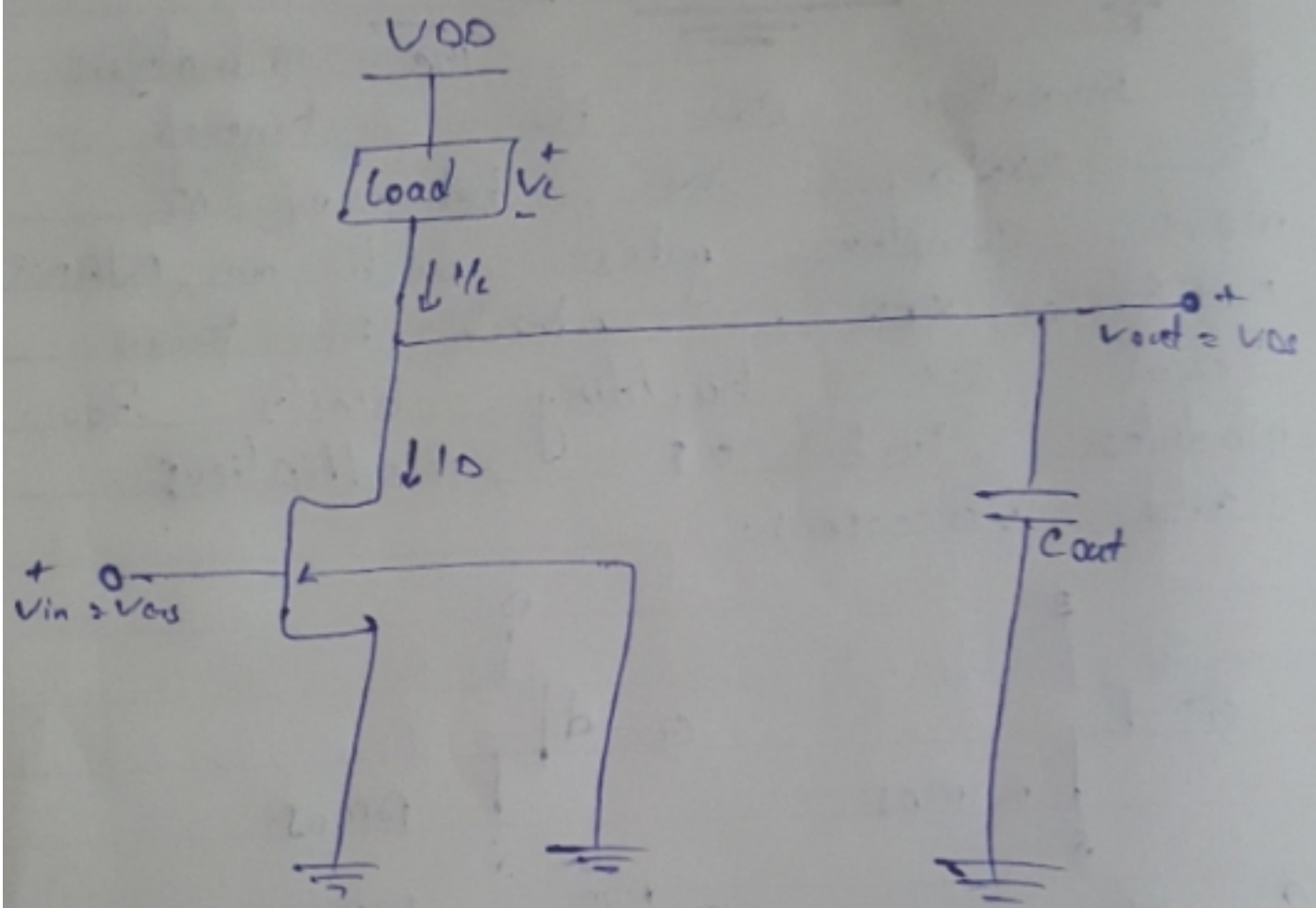
- Sharp V.T.C transition
- better noise margins.
- Single power Supply.
- Smaller overall layout area
- Reduce Standby (leakage) Current.

(*) **Circuit Structure of NMOS.**

Input voltage Vin = VGS.
Out Put voltage Vout = VDS.
Ground VSB = 0

* **Load device:** Terminal current 'I'
Terminal voltage V

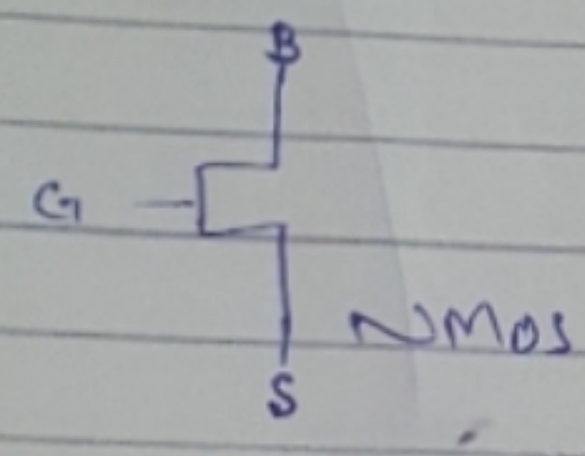
NMOS Diagram:



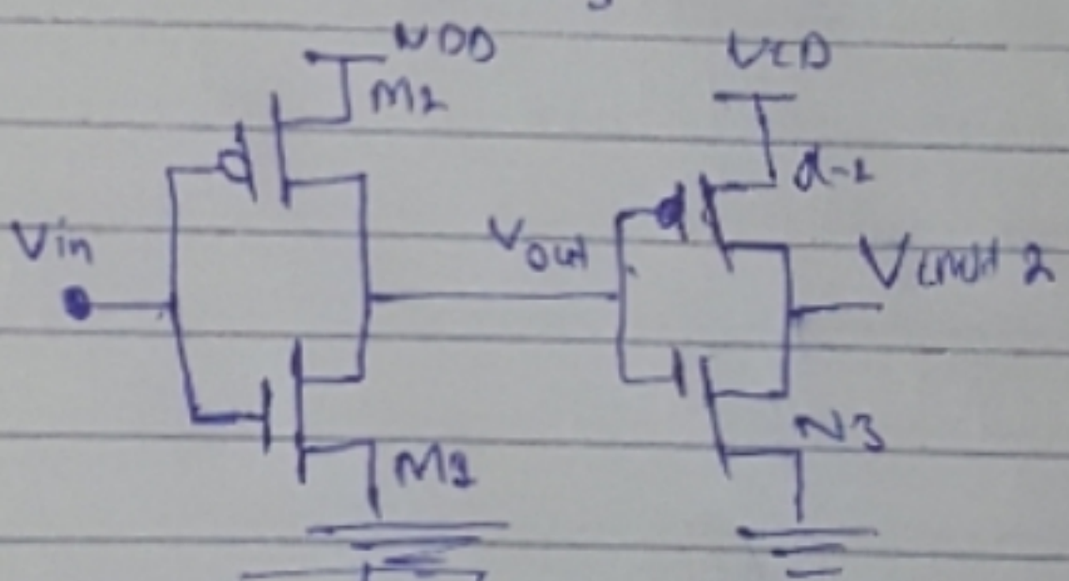
Question (03)

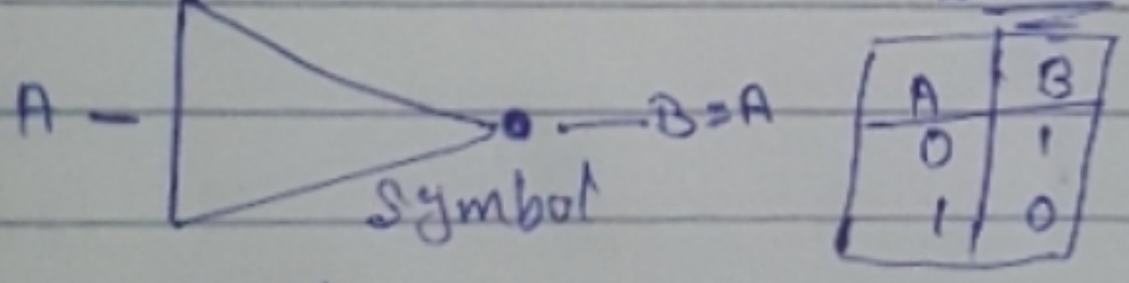
Ans/ # MOS INVERTER #

The analysis of inverter can be extended to explain the behavior of more complex gates such an NAND, NOR, or XOR, which in turn from the building blocks for modules such as Multipliers and processors.

* 

② Circuit

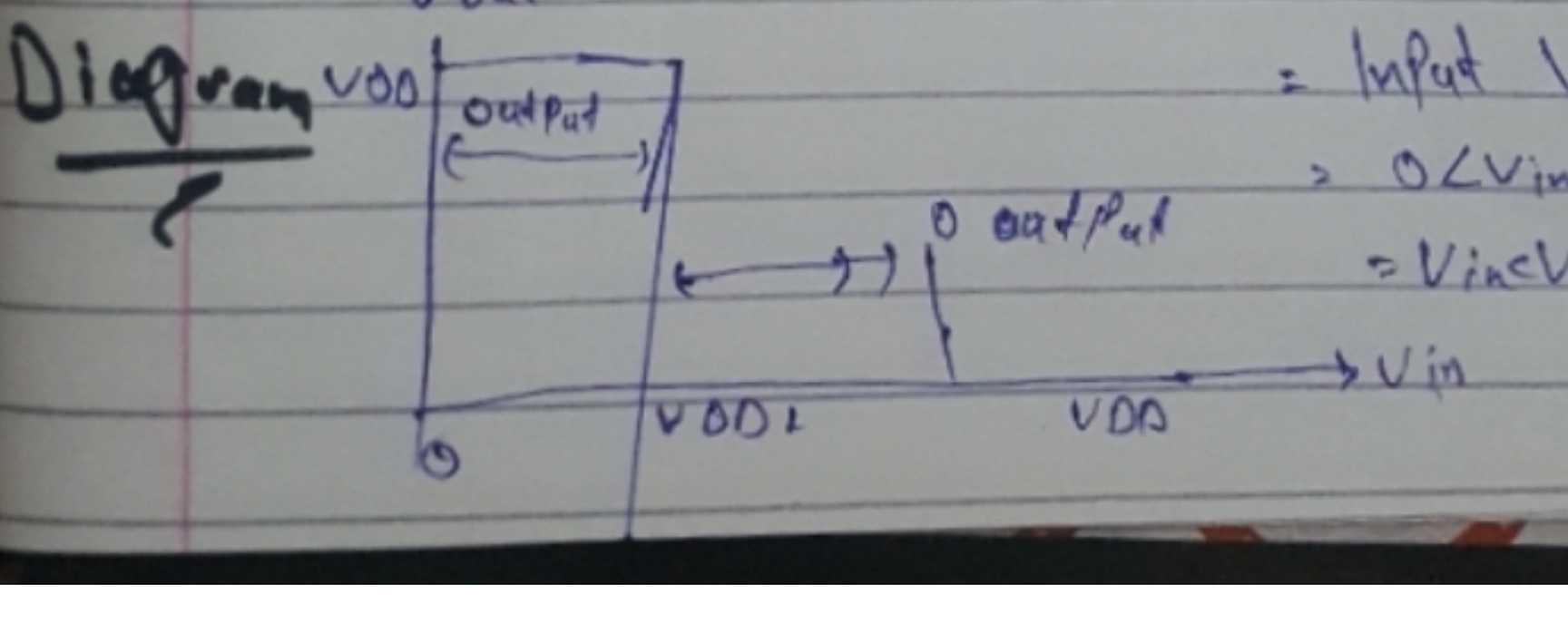




A	B
0	1
1	0

1 represent hig voltage.
Truth Table. 0 Represent Low Voltage.

Diagram



= Input Voltage
= 0 < Vin < Vin => output VDD
= Vin < Vin < VDD output 0.

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Q1 Resistive load Inverter Circuit.

Ans Solution.

(i) $V_{OH} = V_{DD}$

$[V_{OH} = 5V]$

(ii) $V_{OL} = V_{DD} - V_T + \frac{1}{k_n R_L}$ -

$\sqrt{(V_{DD} - V_T + \frac{1}{k_n R_L})^2}$

$= \frac{2 V_{DD}}{k_n R_L}$

* $k_n = k_n' \frac{W}{L}$

$= 20 \times 10^{-6} \times 2$

$k_n = 40 \times 10^{-6}$

* $V_{OL} = 5 - 0.8 + \frac{1}{40 \times 10^{-6} \times 800 \times 10^3} - \sqrt{(5 - 0.8 + \frac{1}{40 \times 10^{-6} \times 800 \times 10^3})^2}$

$= \frac{2 \times 5}{40 \times 10^{-6} \times 800 \times 10^3}$

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$V_{OL} = 4.385 - 2.174$

$\boxed{V_{OL} = 2.151\ V}$

(B) $V_{IL} = V_T + \frac{1}{40\times10^{-6}\times200\times10^{3}}$

$V_{IL} = 0.925$

(*) $V_{IH} = V_T + \sqrt{\frac{8}{3}\frac{V_{DD}}{1mR_L} - \frac{1}{1mR_L}}$

$= 0.8\sqrt{\frac{8}{3}\times\frac{5}{40\times10^{-6}\times200\times10^{3}} - \frac{1}{40\times10^{-6}\times200\times10^{3}}}$

$= 0.8 + 1.289 - 0.125$

$\boxed{V_{IH} = 1.96V}$

* Noise Margin

$N_L = V_{IL} - V_{OL}$

$= 0.925 - 2.15$

$\boxed{N_L = -1.225}$

(*) $N_H = V_{OH} - V_{IH}$

$= 5 - 1.289$

$\boxed{N_H = 3.711}$

Ans)

Q 02

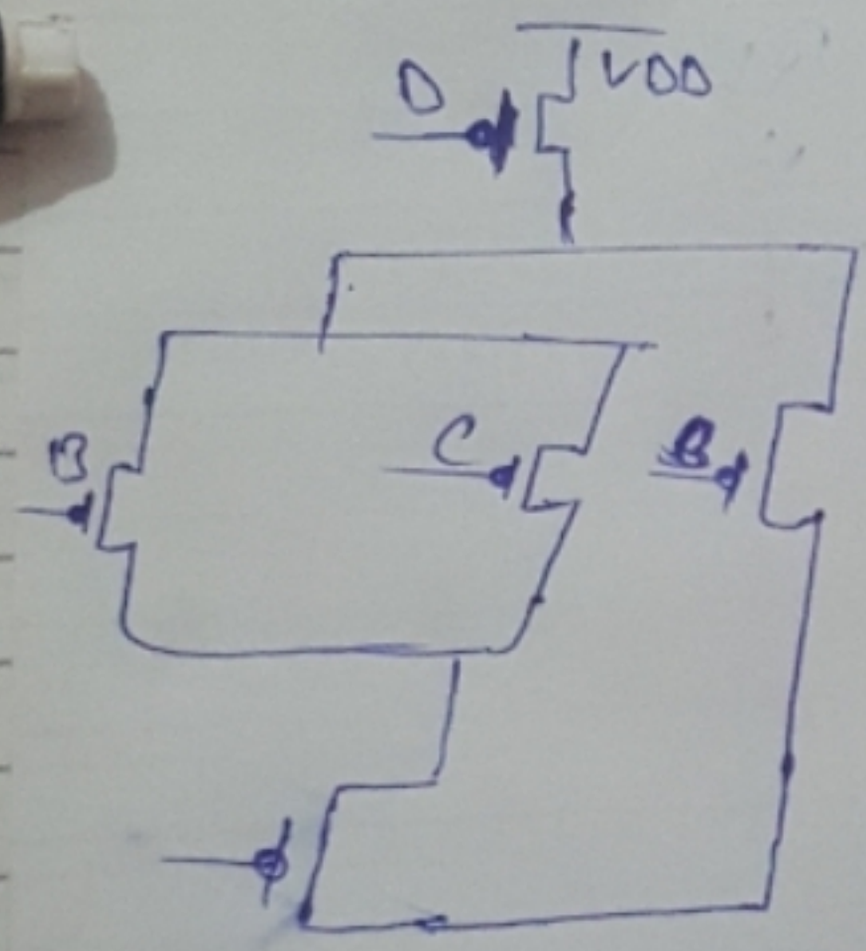
Cmos Logic Layout

$$F = (AB + C)B + D$$

Solution:

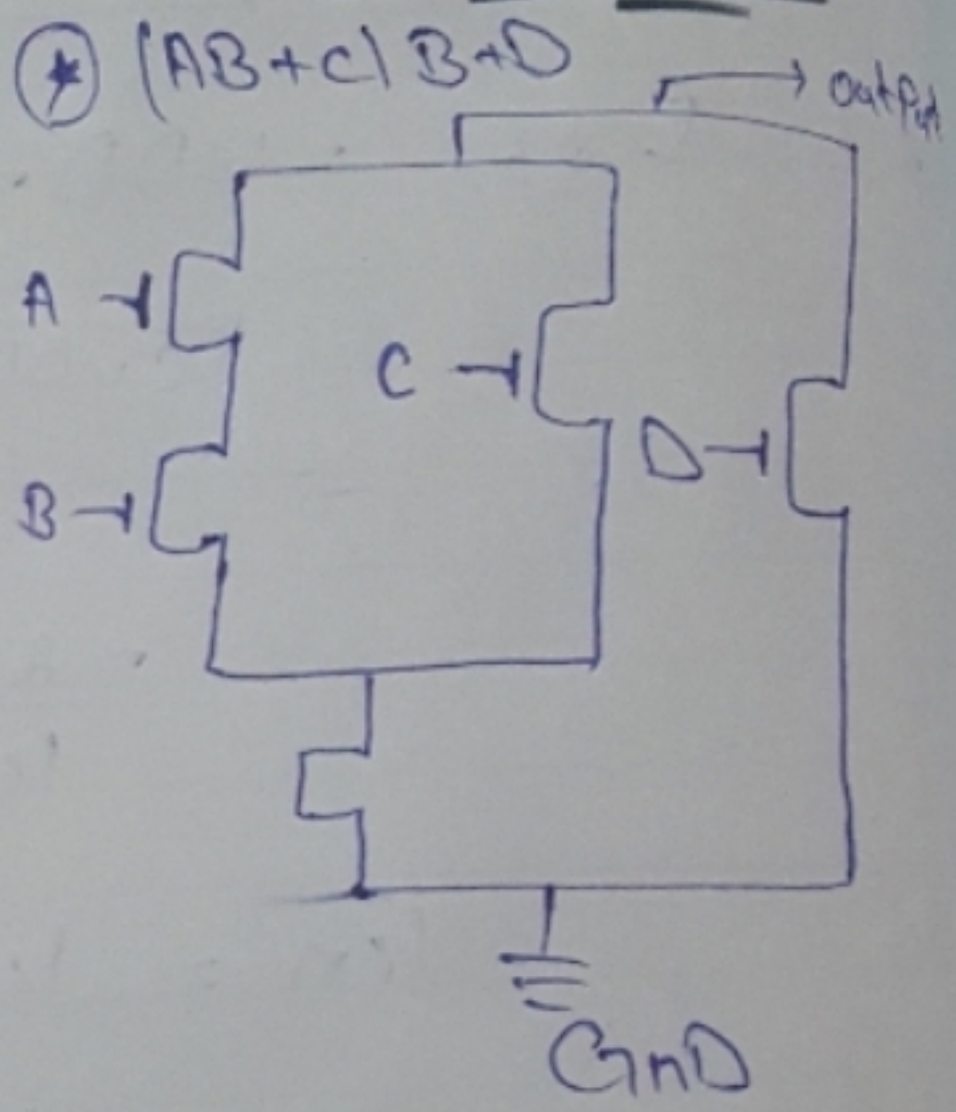
Pull up Network

$$\left[\left[\bar{A}(\bar{B}+\bar{C})\right]+\bar{B}\right]\cdot\bar{D}$$



① Pull down network

$$(AB + C)B + D$$



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